

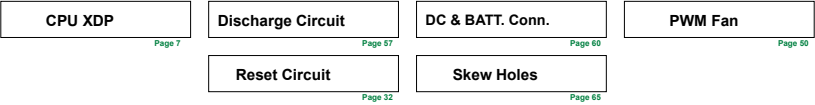
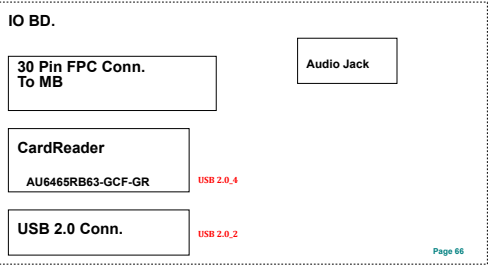
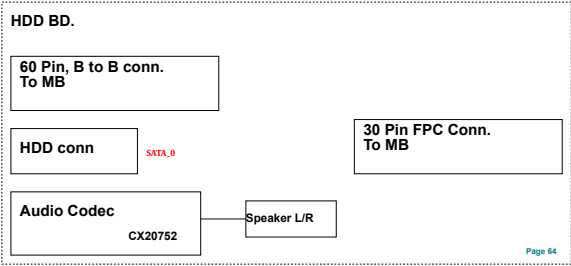
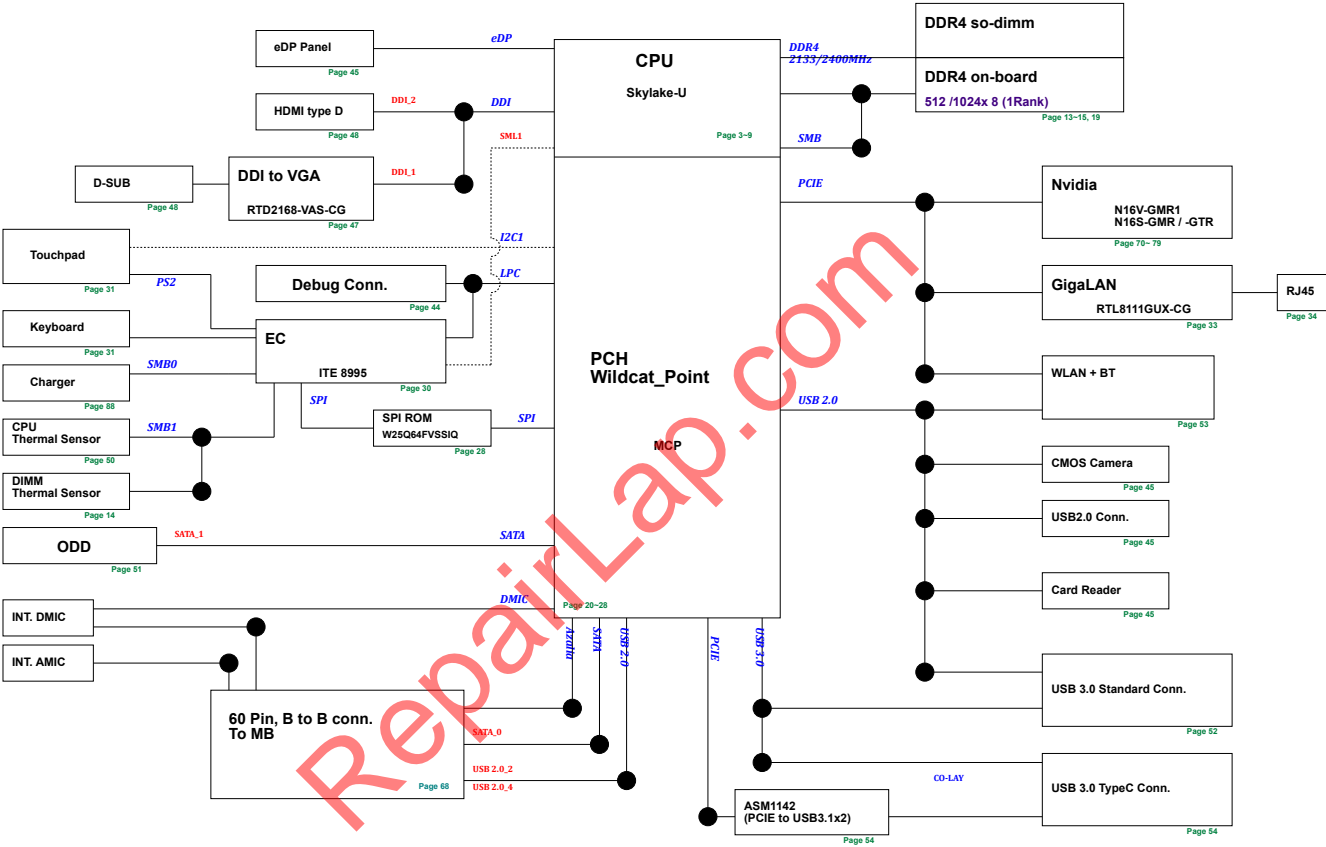
PAGE	Content
001_Block Diagram	
002_System Setting	
003_CPU_DISPLAY	
004_CPU_DDR3	
005_CPU_LPC,SPI,SMB,CLINK	
006_CPU_POEWR	
008_CPU_MISC,JTAG	
009_CPU_CFG,RSVD	
010_CPU_POWER_CAP	
013_DDR3L_TERMINATION	
014_DDR3L_ON-BOARD_A(1)	
015_DDR3L_ON-BOARD_A(2)	
016_DDR3L_SO-DIMM_B	
019_DDR3L_CA_DQ_VOLTAGE	
020_CPU_PCH_CSI2,EMMC	
021_CPU_PCH_CGPIIO, LP10, MISC	
022_CPU_PCH_AUDIO,SDIO,SDXC	
023_CPU_PCH_PCIE,USB,SATA	
024_CPU_PCH_CLOCK SIGNALS,RTC	
025_CPU_PCH_SYS_POWER	
026_CPU_PCH_POEWR,GND	
027_CPU_PCH_POEWR,GND	
028_PCH-SPI ROM,OTH	
030_KBC_KB9026QC	
031_KBC_KB,TP	
032_RST_Reset Circuit	
033_LAN_RTL8111GUX-CG	
034_LAN_RJ45	
044_DEBUG PORT	
045_CRT_LCD Panel_CMOS_DMIC	
047_eDP to VGA & CRT D-SUB	
048_HDMI-type D	
050_FAN & SENSOR	
051_SATA_ODD	
052_USB 3.0 CONNECTOR	
053_MINICARD (WLAN)	
056_PWR_BTN & LID_SW	
057_DSG_Discharge	
058_PRO_Protect	
060_DC_DC & BAT_IN	
064_BD_HDD_SATA	
065_SCREW HOLE, SMT NUT	
066_DB_IO USB*2 & CR & LED	
067_MB_LED	
068_B to B connector	
069_EMI	
070_VGA_nVIDIA_N16V/S_PCIE	
071_VGA_nVIDIA_N16V/S_FB-IF	
072_VGA_nVIDIA_N16V/S_FB-DDR3	
073_VGA_nVIDIA_N16V/S_VDD	
074_VGA_nVIDIA_N16V/S_DISPLAY	
075_VGA_nVIDIA_N16V/S_ROM,XTAL	
076_VGA_nVIDIA_N16V/S_GPIO	
077_VGA_nVIDIA_N16V/S_POWER	

080_PW_IMVP8 (1) (RT3601BCGQW)
081_PW_IMVP8 (2) (RT3601BCGQW)
083_PW_+1.0VSUS / +1.8VSUS
084_PW_+1.2VSUS/+1.2V
086_PW_1.35V/+0.675VS (UP9011Q)
087_PW_+3VADSW/+5VSUS (RT8249C)
088_PW_LOAD SWITCH
089.PW_CHARGER(BQ24780)
090_PW_PROTECTION
091_PW_DGPU_2PHASE(RT8815A)

# X556 SCHEMATIC Revision 1.0

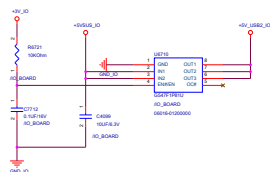
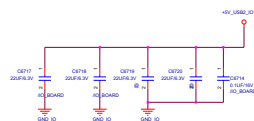
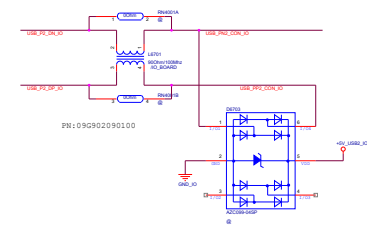
(UAM:UMA)  
(UV : DGPU = Nvidia N16V-GMR1)  
(UR : DGPU = Nvidia N16S-GMR)  
(UQ : DGPU = Nvidia N16S-GTR)

Non Connected Standby

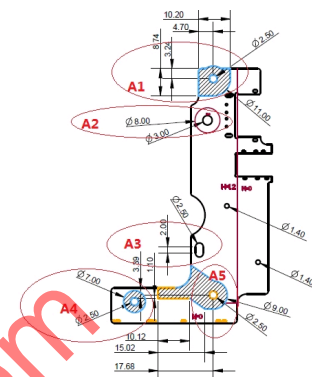
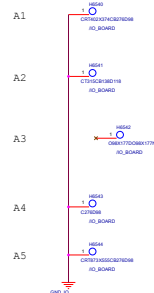
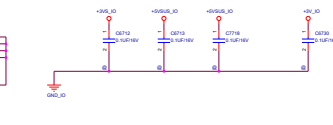
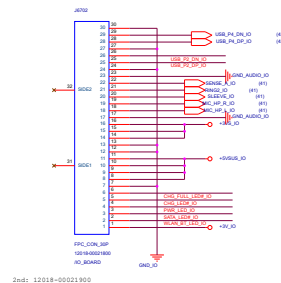
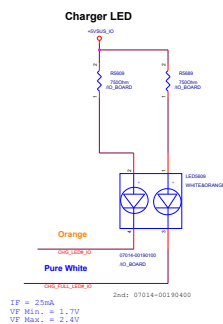


PCB_ITEM_REF	Dev As	Signal Name	Power on Default State	IO & E2C Pull-up (open)	Power	PCB_ITEM_REF	Dev As	Signal Name	Power on Default State	IO & E2C Pull-up (open)	Power
EXP_A0	Native	CK_DIV		500 KΩ 100	1V0V	EXP_020	GPIO	N/A			
EXP_A1	Native	LPC_A00			1V0V	EXP_021	GPIO	SHARED_SIGNAL_INTERRUPT_A0	N/A	500 KΩ 100	1V0V
EXP_A2	Native	LPC_A01			1V0V	EXP_022	GPIO	ARM_VIO_INTERRUPT_A1	N/A	500 KΩ 100	1V0V
EXP_A3	Native	LPC_A02			1V0V	EXP_023	GPIO	ARM_VIO_INTERRUPT_A2	N/A	500 KΩ 100	1V0V
EXP_A4	Native	LPC_A03			1V0V	EXP_024	GPIO	N/A			
EXP_A5	Native	LPC_FNAME0			1V0V	EXP_025	GPIO	ARM_INTERRUPT_A3	N/A		1V0V
EXP_A6	Native	INT_INTERRUPT		500 KΩ 100	1V0V	EXP_026	GPIO	ARM_INTERRUPT_INTERRUPT_A4	N/A		1V0V
EXP_A7	GPIO	N/A				EXP_027	GPIO	N/A			
EXP_A8	Native	FW_CLOCKING		500 KΩ 100	1V0V	EXP_028	Native	ARM_INTERRUPT_INTERRUPT_A5		500 KΩ 100	1V0V
EXP_A9	Native	GPIO_INTERRUPT_PIN			1V0V	EXP_029	Native	GPIO_INTERRUPT_INTERRUPT_A6		500 KΩ 100	1V0V
EXP_A10	Native	CLK_DIV00			1V0V	EXP_030	Native	GPIO_INTERRUPT_INTERRUPT_A7		500 KΩ 100	1V0V
EXP_A11	GPIO	N/A				EXP_031	GPIO	GPIO_INTERRUPT_INTERRUPT_A8		500 KΩ 100	1V0V
EXP_A12	GPIO	N/A				EXP_032	GPIO	GPIO_INTERRUPT_INTERRUPT_A9		500 KΩ 100	1V0V
EXP_A13	Native	GPIO_INTERRUPT		500 KΩ 100	1V0V	EXP_033	GPIO	GPIO_INTERRUPT_INTERRUPT_A10		500 KΩ 100	1V0V
EXP_A14	Native	GPIO_INTERRUPT		500 KΩ 100	1V0V	EXP_034	Native	GPIO_INTERRUPT_INTERRUPT_A11		500 KΩ 100	1V0V
EXP_A15	Native	GPIO_INTERRUPT				EXP_035	Native	GPIO_INTERRUPT_INTERRUPT_A12		500 KΩ 100	1V0V
EXP_A16	GPIO	N/A				EXP_036	GPIO	GPIO_INTERRUPT_INTERRUPT_A13		500 KΩ 100	1V0V
EXP_A17	GPIO	N/A				EXP_037	GPIO	GPIO_INTERRUPT_INTERRUPT_A14		500 KΩ 100	1V0V
EXP_A18	GPIO	N/A				EXP_038	Native	GPIO_INTERRUPT_INTERRUPT_A15		500 KΩ 100	1V0V
EXP_A19	GPIO	N/A				EXP_039	Native	GPIO_INTERRUPT_INTERRUPT_A16		500 KΩ 100	1V0V
EXP_A20	GPIO	N/A				EXP_040	Native	GPIO_INTERRUPT_INTERRUPT_A17		500 KΩ 100	1V0V
EXP_A21	GPIO	N/A				EXP_041	Native	GPIO_INTERRUPT_INTERRUPT_A18		500 KΩ 100	1V0V
EXP_A22	GPIO	N/A				EXP_042	Native	GPIO_INTERRUPT_INTERRUPT_A19		500 KΩ 100	1V0V
EXP_A23	GPIO	N/A				EXP_043	Native	GPIO_INTERRUPT_INTERRUPT_A20		500 KΩ 100	1V0V
EXP_B0	GPIO	N/A (VIO_INTERRUPT)		500 KΩ 100	1V0V	EXP_044	GPIO	N/A			
EXP_B1	GPIO	N/A (VIO_INTERRUPT)		500 KΩ 100	1V0V	EXP_045	GPIO	N/A			
EXP_B2	GPIO	N/A				EXP_046	GPIO	N/A			
EXP_B3	GPIO	N/A				EXP_047	GPIO	N/A			
EXP_B4	GPIO	N/A				EXP_048	GPIO	N/A			
EXP_B5	Native	CLK_DIV00	GPIO CLK REQUEST	500 KΩ 100	1V0V	EXP_049	GPIO	N/A			
EXP_B6	GPIO	N/A				EXP_050	GPIO	N/A			
EXP_B7	GPIO	N/A				EXP_051	GPIO	N/A			
EXP_B8	GPIO	N/A				EXP_052	GPIO	N/A			
EXP_B9	Native	CLOCKING_CLOCK	GPIO CLK REQUEST	500 KΩ 100	1V0V	EXP_053	GPIO	N/A			
EXP_B10	Native	CLOCKING_CLOCK	GPIO CLK REQUEST	500 KΩ 100	1V0V	EXP_054	GPIO	N/A			
EXP_B11	Native	GPIO_INTERRUPT	GPIO CLK REQUEST	500 KΩ 100	1V0V	EXP_055	GPIO	N/A			
EXP_B12	Native	GPIO_INTERRUPT	GPIO CLK REQUEST	500 KΩ 100	1V0V	EXP_056	GPIO	N/A			
EXP_B13	Native	GPIO_INTERRUPT	GPIO CLK REQUEST	500 KΩ 100	1V0V	EXP_057	GPIO	N/A			
EXP_B14	GPIO	N/A				EXP_058	GPIO	N/A			
EXP_B15	GPIO	N/A				EXP_059	GPIO	N/A			
EXP_B16	GPIO	N/A				EXP_060	GPIO	N/A			
EXP_B17	GPIO	N/A				EXP_061	GPIO	N/A			
EXP_B18	GPIO	N/A				EXP_062	GPIO	N/A			
EXP_B19	GPIO	N/A				EXP_063	GPIO	N/A			
EXP_B20	GPIO	N/A				EXP_064	GPIO	N/A			
EXP_B21	GPIO	N/A				EXP_065					

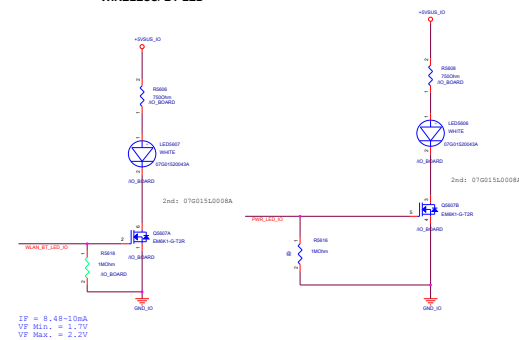
## USB2.0 CONN



## LED indicator



## POWER LED



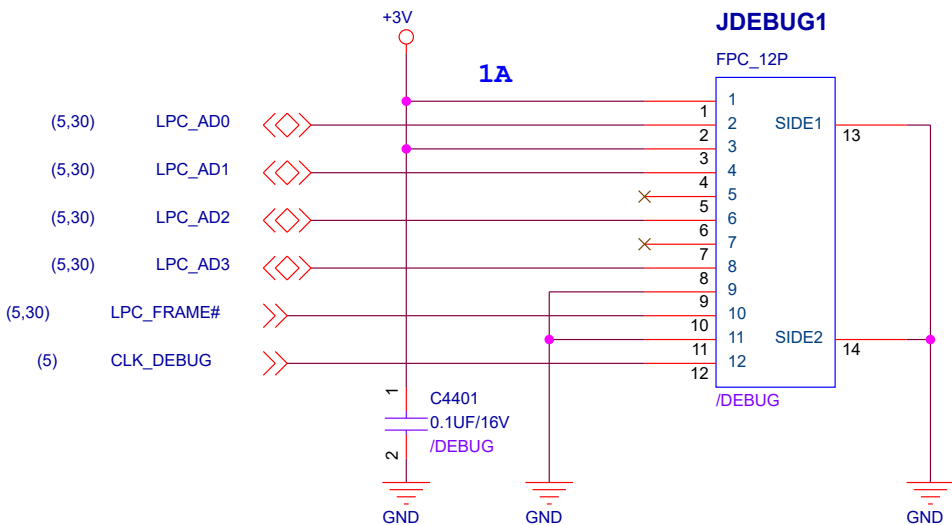
RepairLap.com



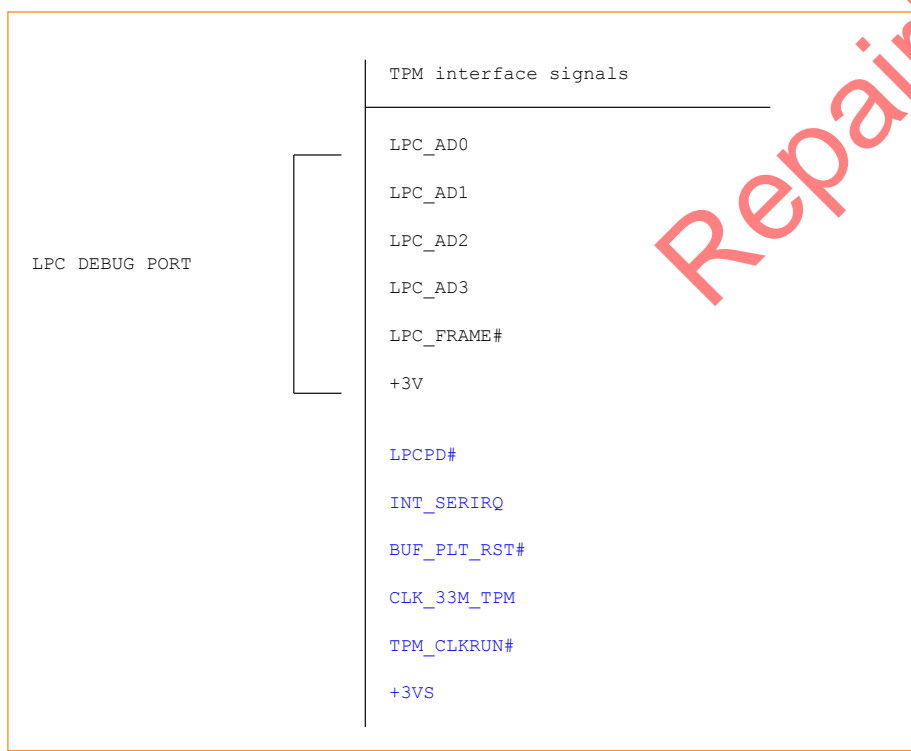




LPC DEBUG PORT



RepairLap.com



BOM

<b>ASUS</b>		Project Name	Rev
		<b>X556UV</b>	R1.0
Title : <b>DEBUG PORT</b>			
Size A	Dept.: <b>ASUSTeK COMPUTER INC.</b> Engineer: <b>EE</b>		
Date: <b>Monday, January 04, 2016</b>	Sheet	44	of 102

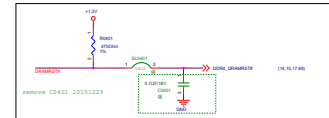
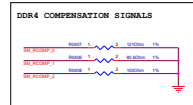


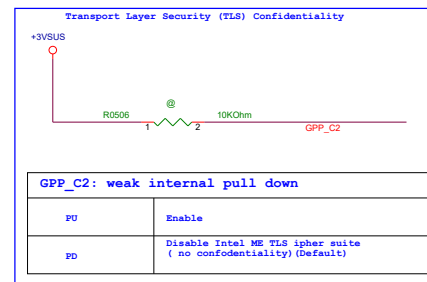
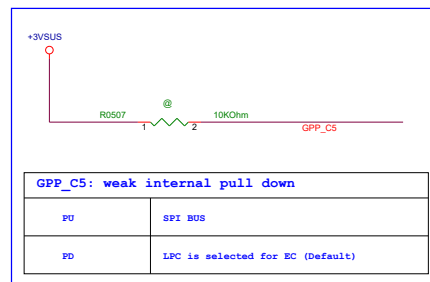
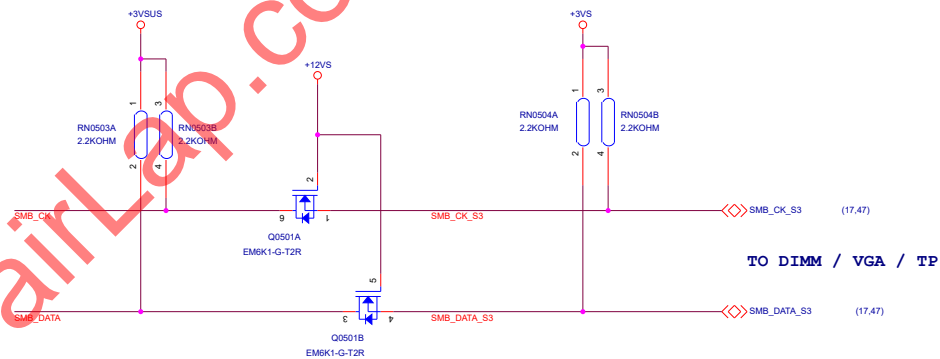
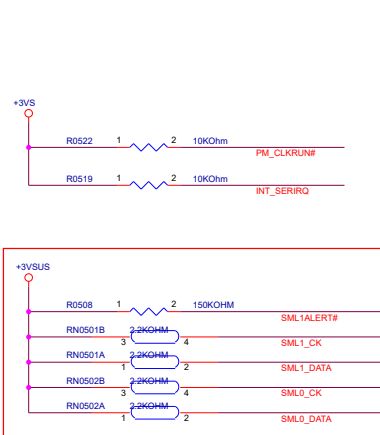
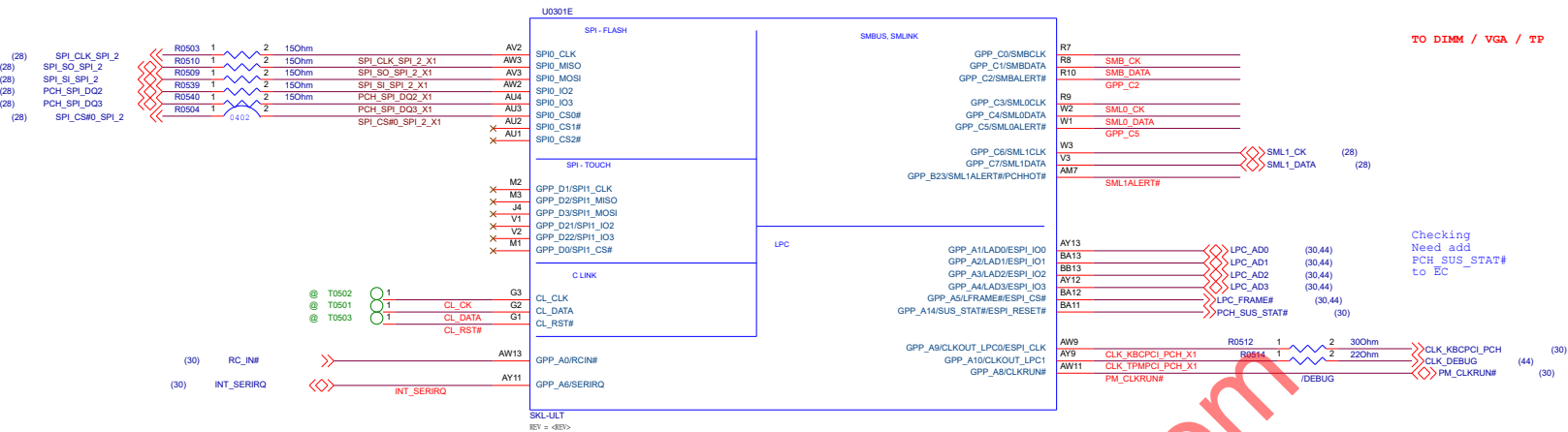
## Memory Channel B



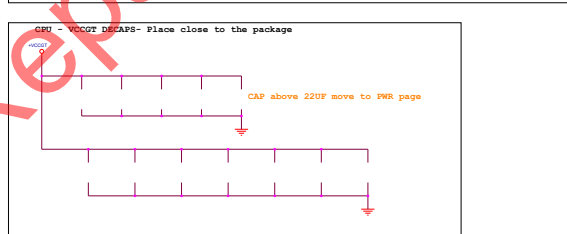
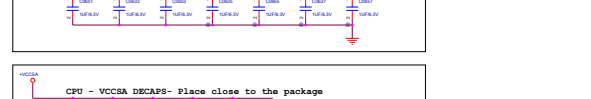
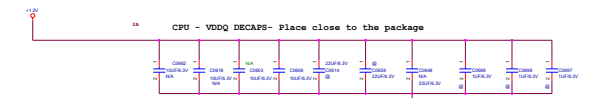
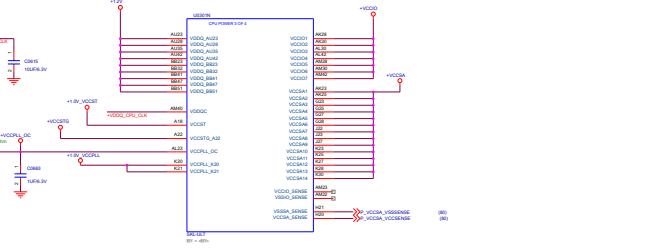
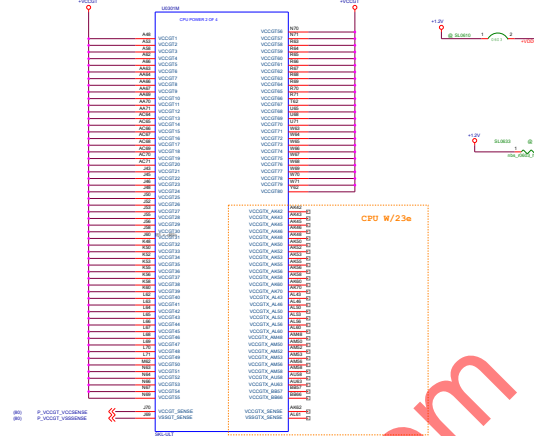
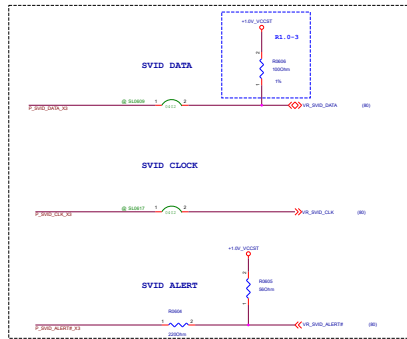
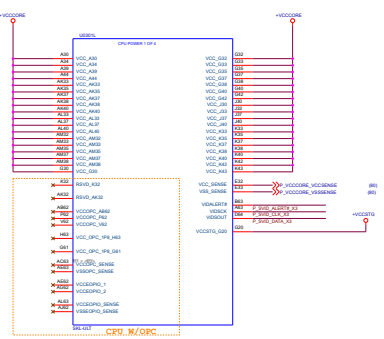
DDR\_VTT\_CTRL:  
System Memory Power Gate Control:  
Disables the platform memory VTT regulator  
in CB and deeper and S3.  
Ref:544924\_544924\_Skylake\_EDS\_Vol\_1\_Rev0.9.pdf P.120

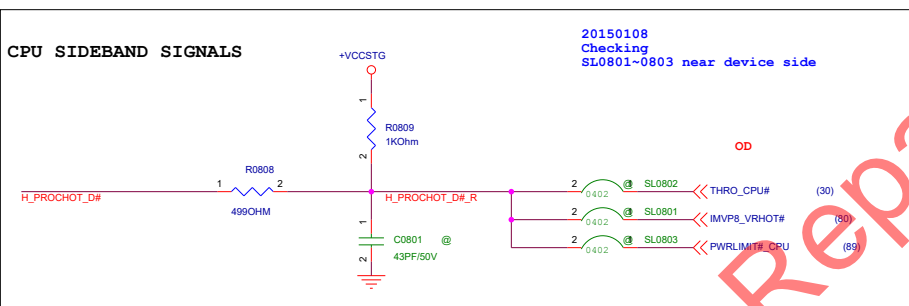
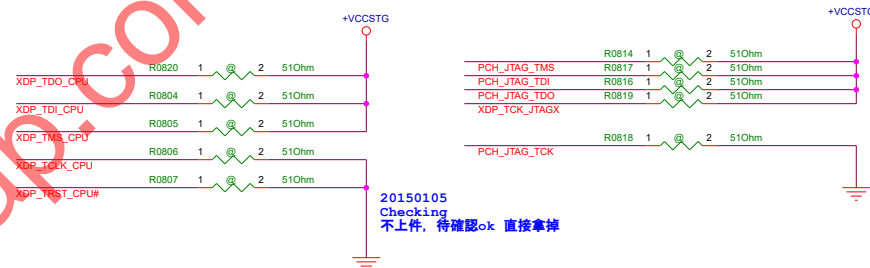
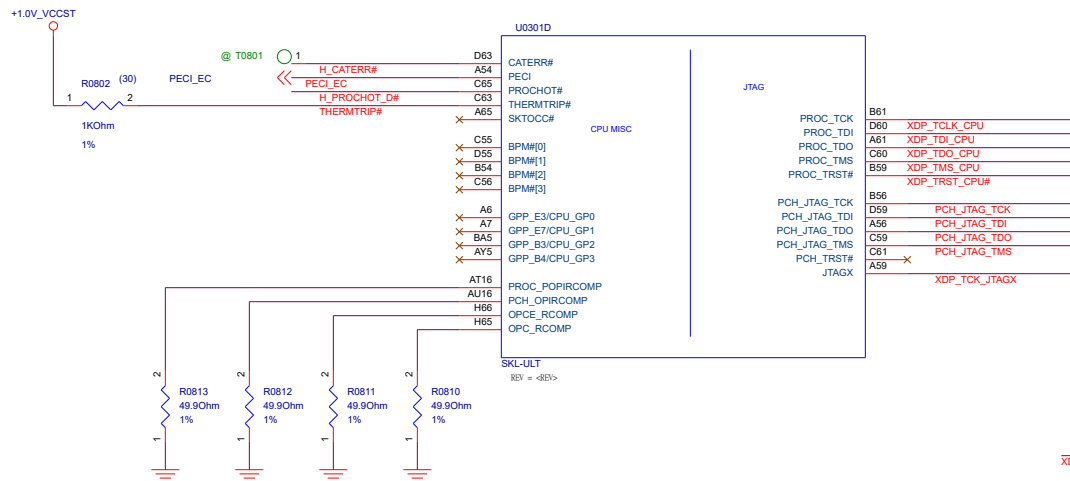
VTT Enable

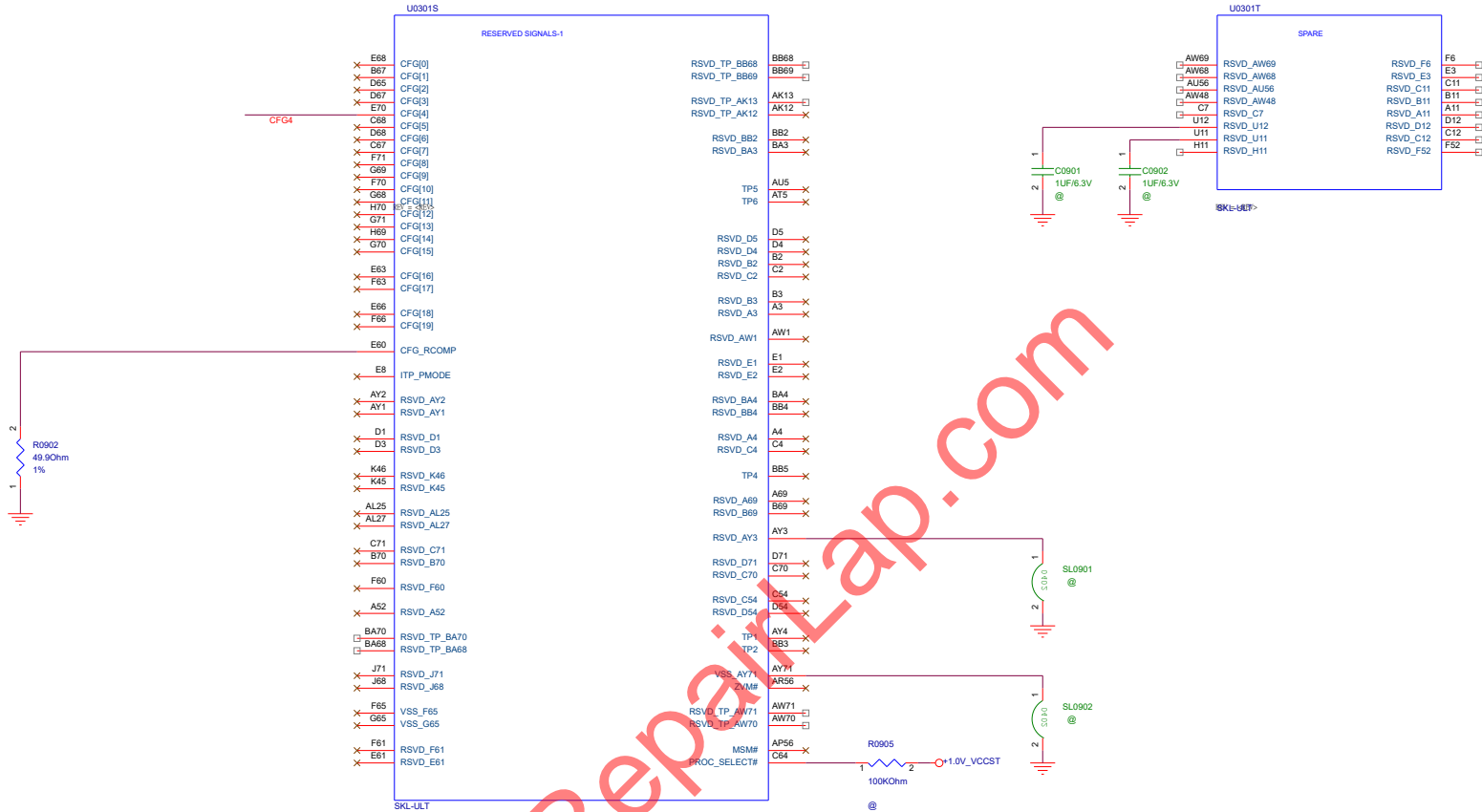




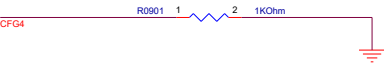
BOM







CFG STRAPS



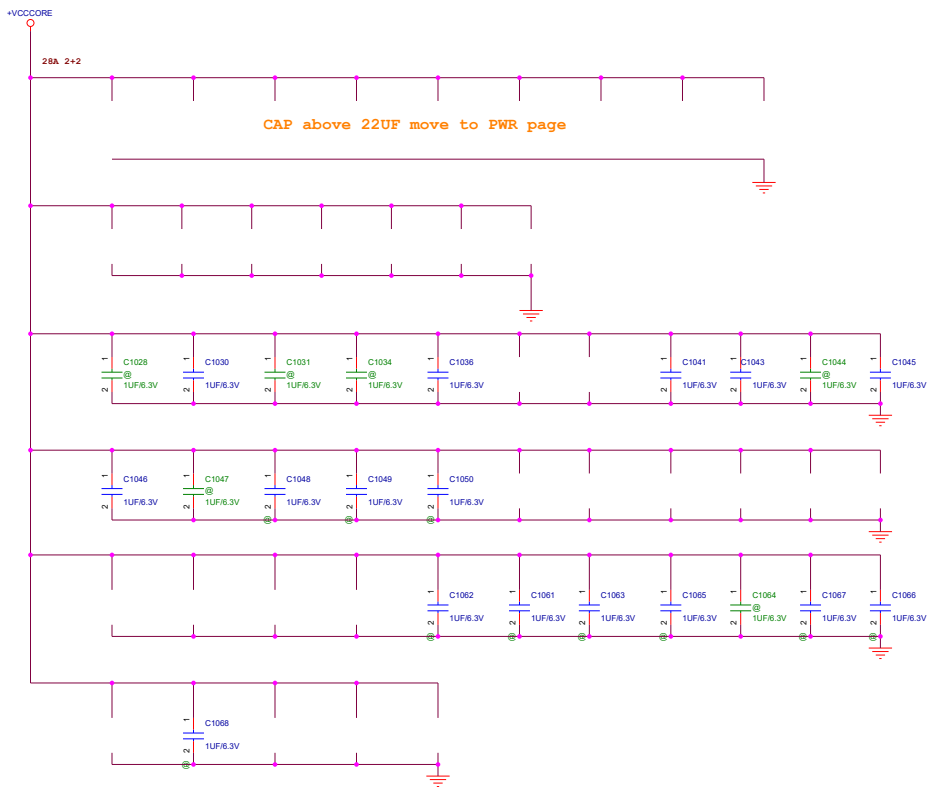
	1	0	NOTE
CFG0	NO STALL	STALL	STALL RESET SEQUENCE AFTER PCU PLL LOCK UNTIL DE-ASSERTED
CFG4	DISABLE	ENABLE	eDP ENABLE

BOM

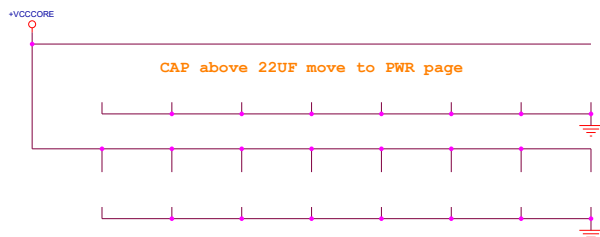
ASUS		Project Name	Rev
		X5560V	R1.0
Title : CPU_CFG.RSVD			
Size	Custom	Dept. : ASUSTek COMPUTER INC.	Engineer: SZ/EE
Date: Monday, January 04, 2016		Sheet 9	of 102



# CPU - VCC DECAPS- Underneath the package



## CPU - VCC DECAPS- Place close to the package



BOM

ASUS		Project Name	Rev
X5560V			R1.0
Title : CPU_POWER_CAP			
Size	Dept.:	ASUSTek COMPUTER INC.	Engineer: SZ/EE
C	Date:	Monday, January 04, 2016	Sheet 10 of 102







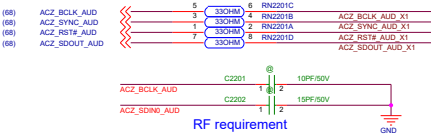






HD Audio

RN2201 near PCH

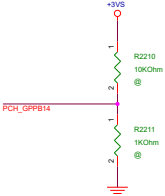


RF requirement

ACZ\_SDOUT:(1) PCH: Internal PD 20k ohm, VIL=0.35V, VIH=0.65~3.3V (2) ALCZ69:VIL<0.35\*3.3V, VIH>0.65\*3.3V

ACZ\_SDOUT is a signal used for Flash Descriptor security Override/MS debug mode HIGH : get overrideen, LOW : disable override

Top Swap Override



PCH_GPPB14: weak internal pull down	
PU	Enable
PD	Disable (default)



Checking  
內建SDIO  
如果Pin 數ok  
(Or connector 在大板上)  
可考慮

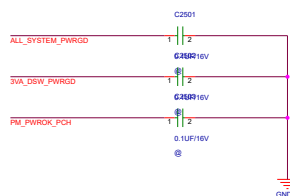
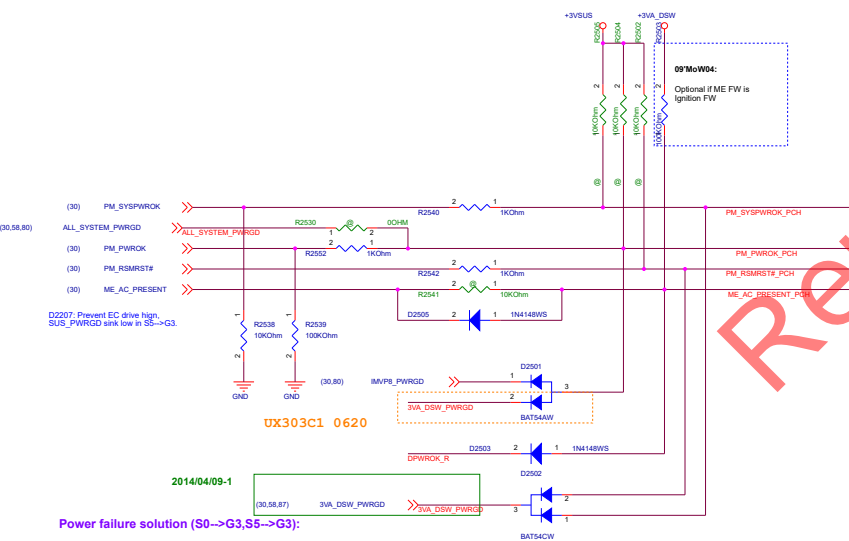
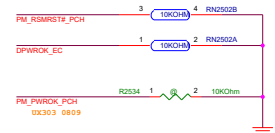
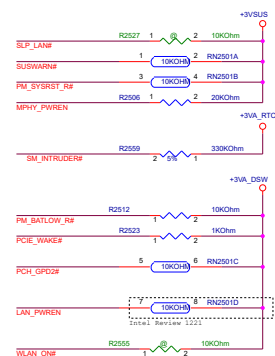
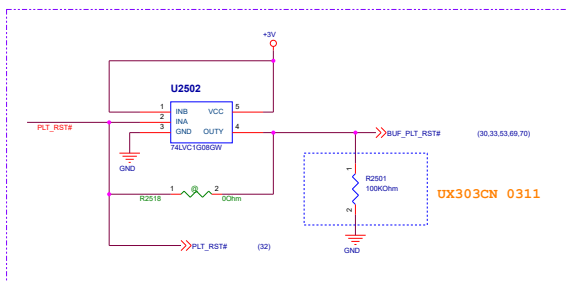
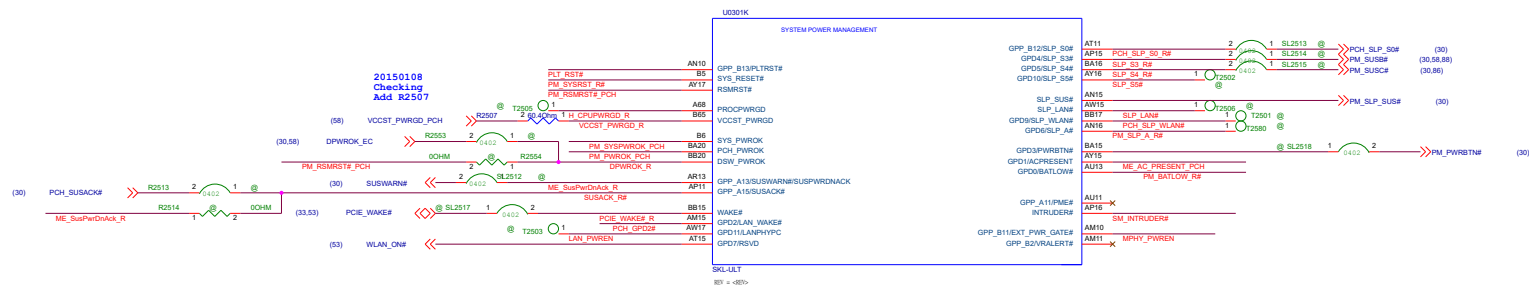
20150105  
Checking  
沒使用是否要 PU /PD ?  
Remove unused function (PU/PD remove)

Checking  
沒使用是否要 PU /PD ?



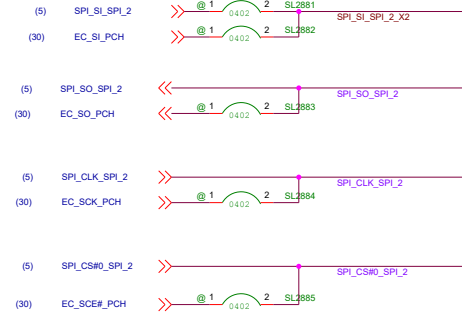






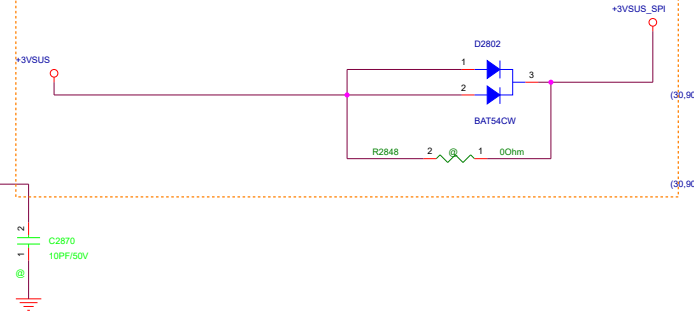


remove ISOLATION

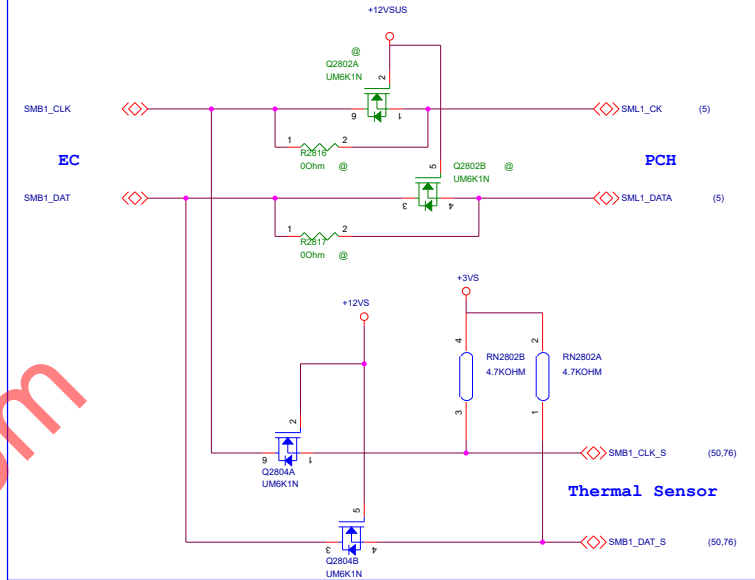


## SPI PCH Power

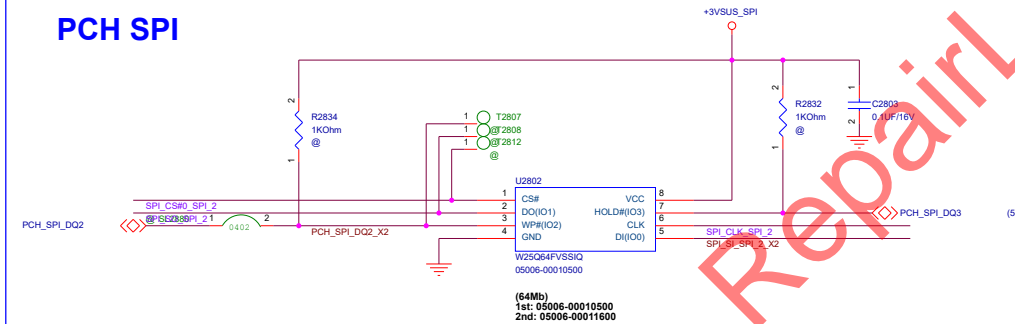
UX303 0814



## System Management Interface

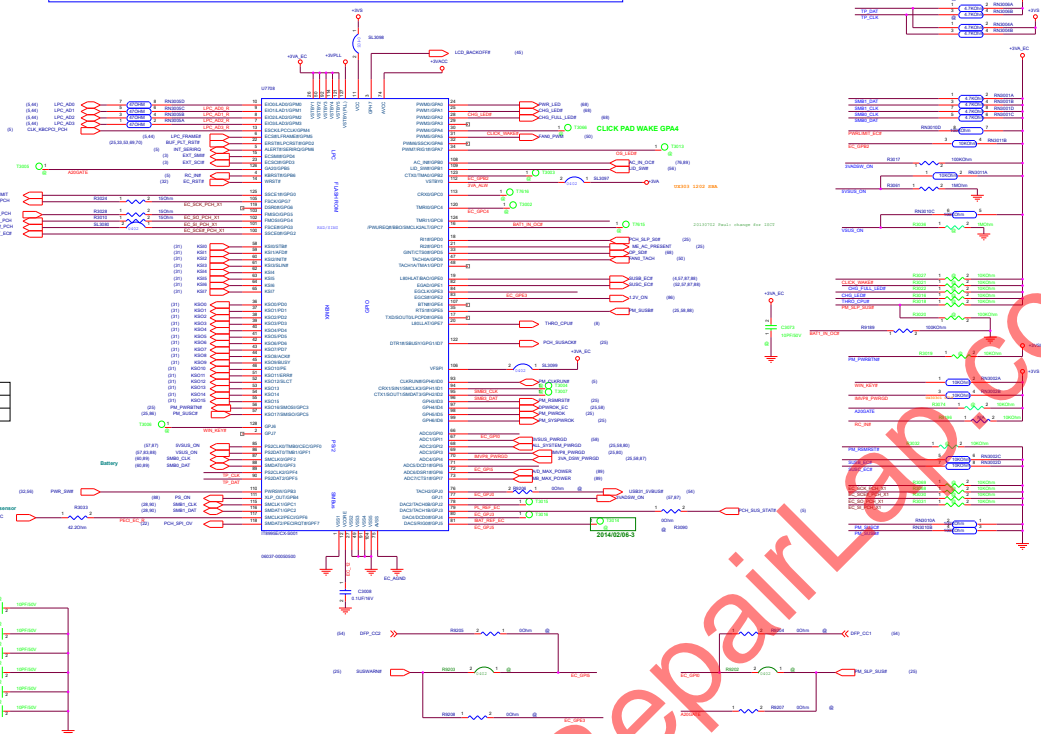


## PCH SPI

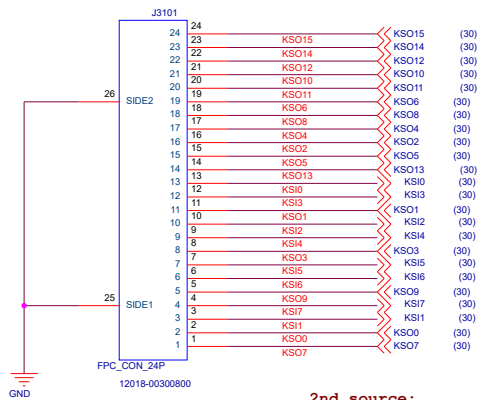


BOB

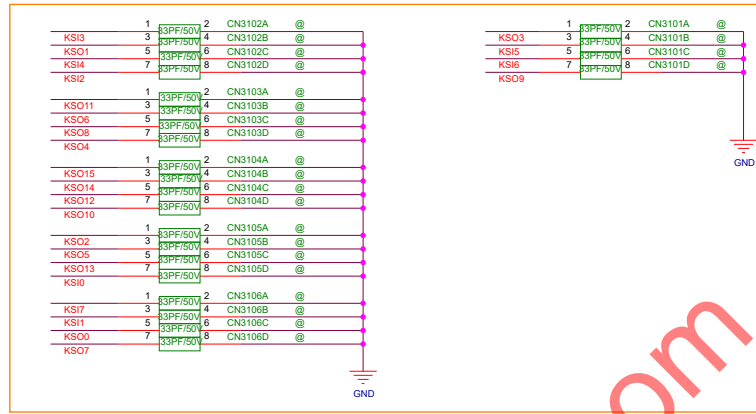
Project Name		Rev
ASUS X556UV		R1.0
Title : PCH-SPI ROM,OTH		
Size	Dept.:	ASUSTek COMPUTER INC. Engineer: EE
A3	Date: Monday, January 04, 2016	Sheet 28 of 102



# Internal Keyboard

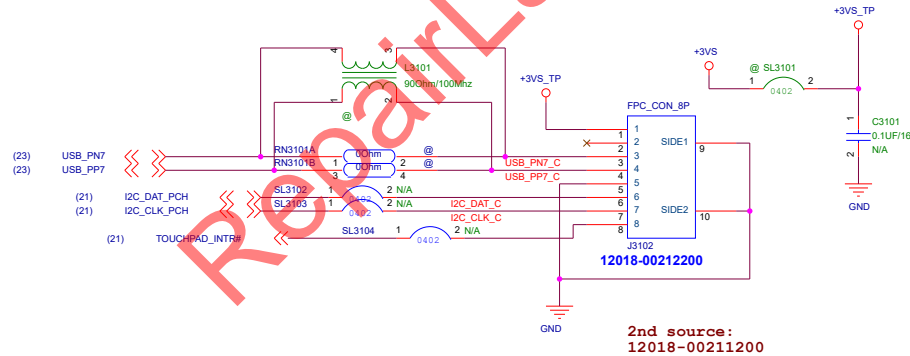


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12018-00301000  
12018-00300000

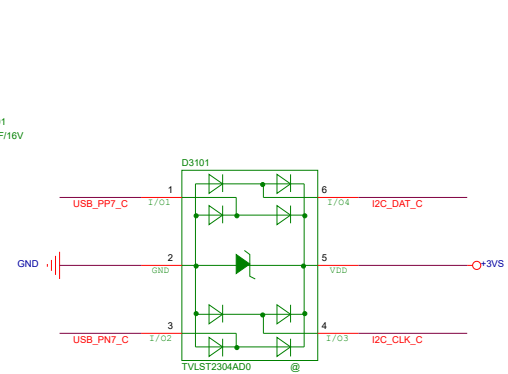


## Touch PAD

Checking  
CPAD\_INT#\_CPU remove  
CPAD\_INT#\_PCH-TOUCHPAD\_INTR#



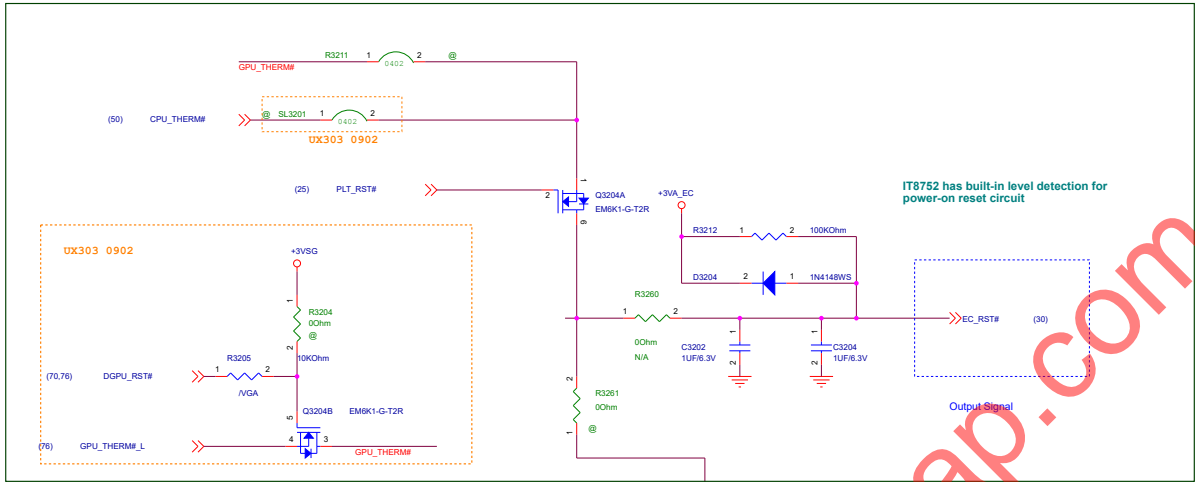
2nd source:  
12018-00212200



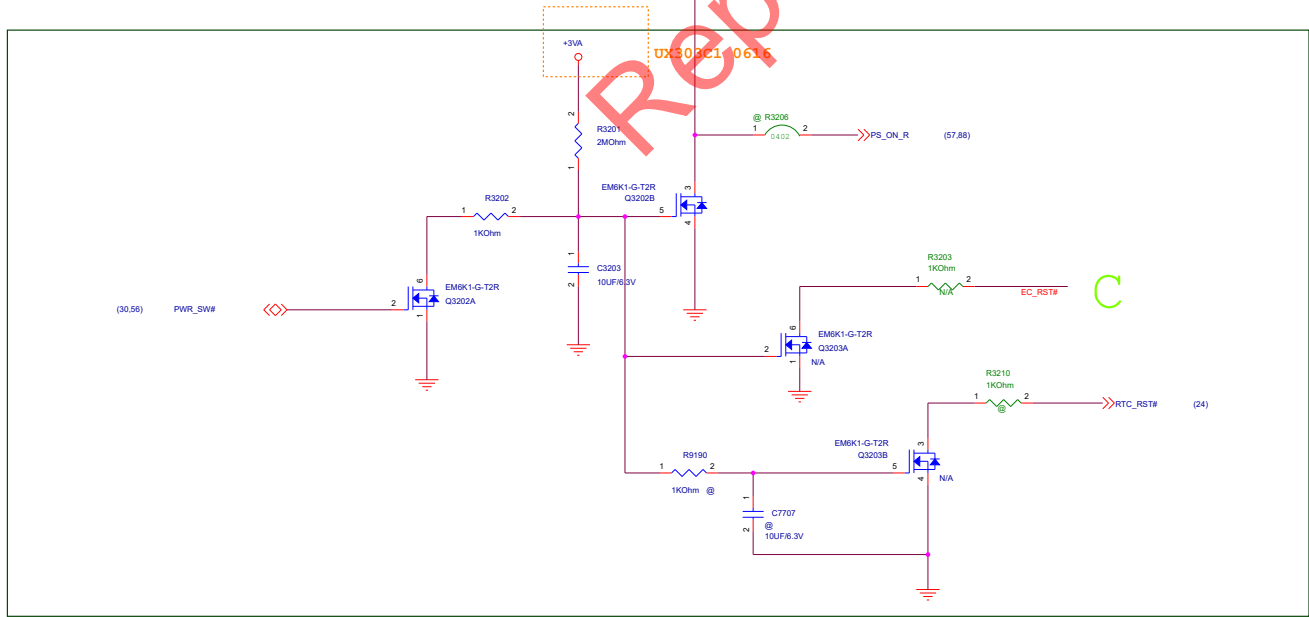
BOM

ASUS		Project Name	Rev
X556UV			R1.0
Title : EC-IT8572(2)_KB,TP			
Size	Dept.:	ASUSTek COMPUTER INC.	Engineer: EE
Date: Monday, January 04, 2016	Sheet	31	of 102

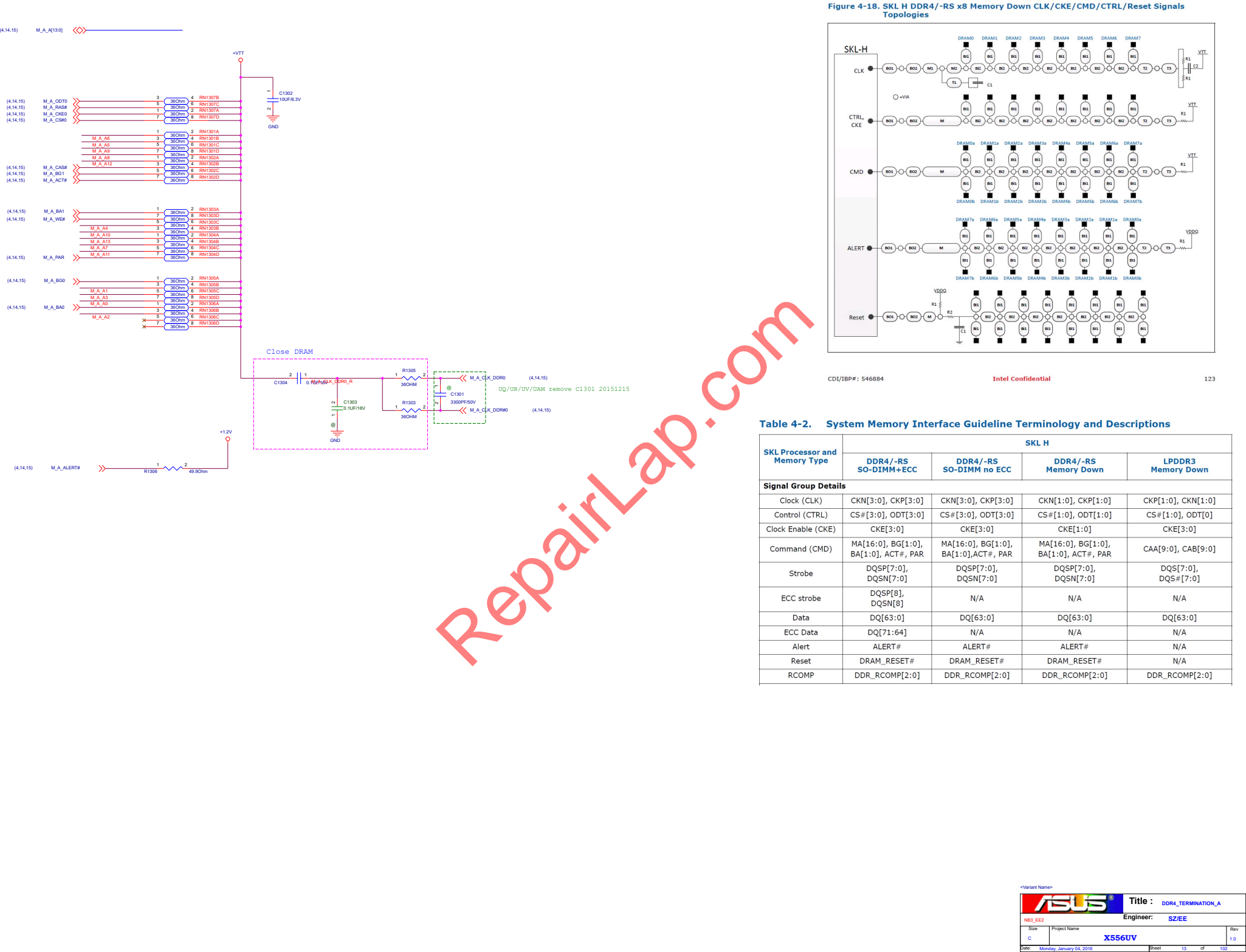
Thermal Policy



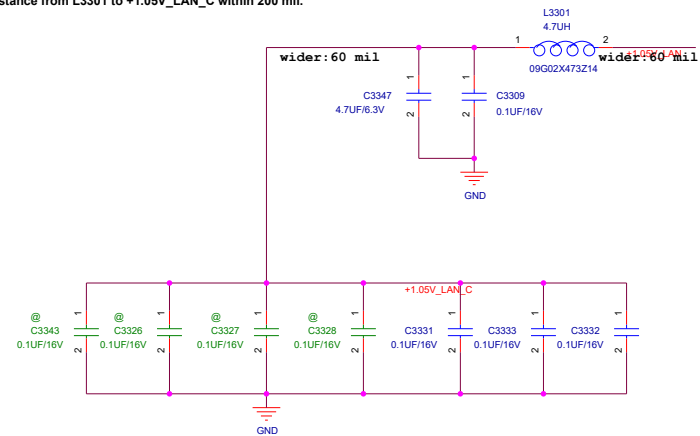
battery embedded (press pwr\_sw 10sec, then reset ec )



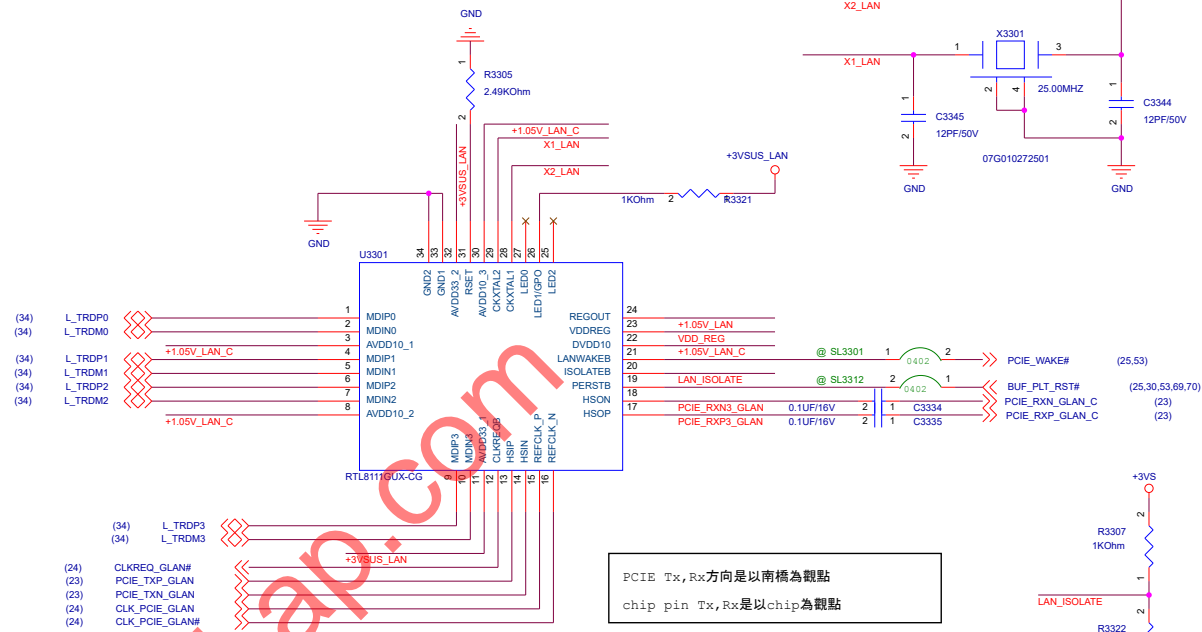
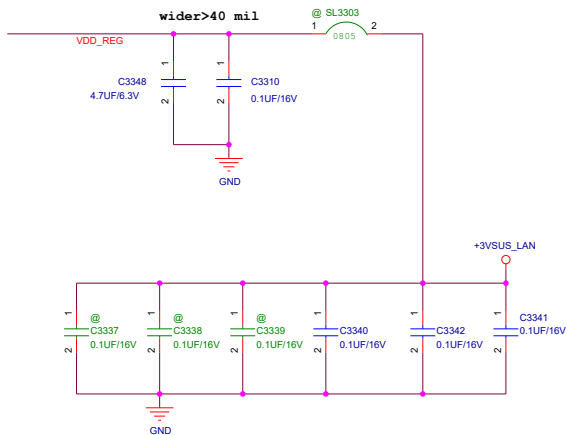




The distance from u3301.36 to L3301 within 200 mil.



The distance from U3301.34, U3301.35, VDD\_REG net to SL3303 within 200 mil.



RTK建議3V\_LAN raise time >0.5ms

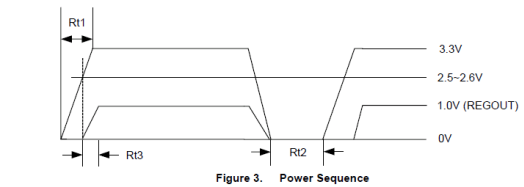
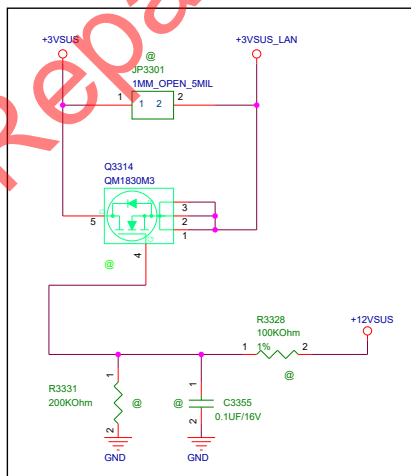
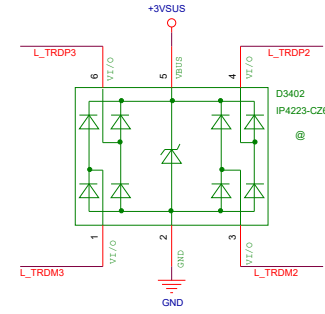
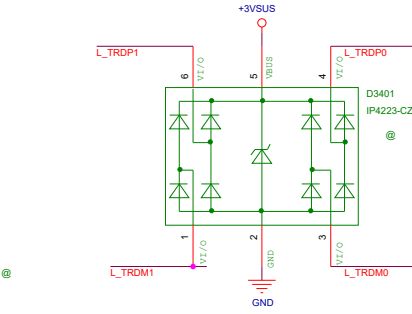
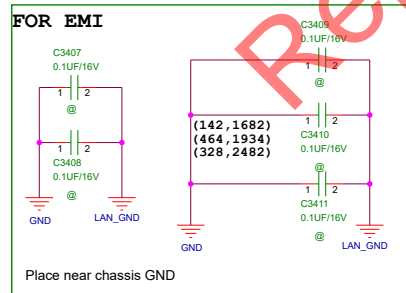
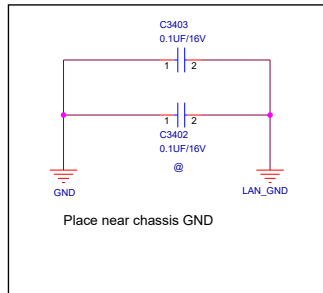
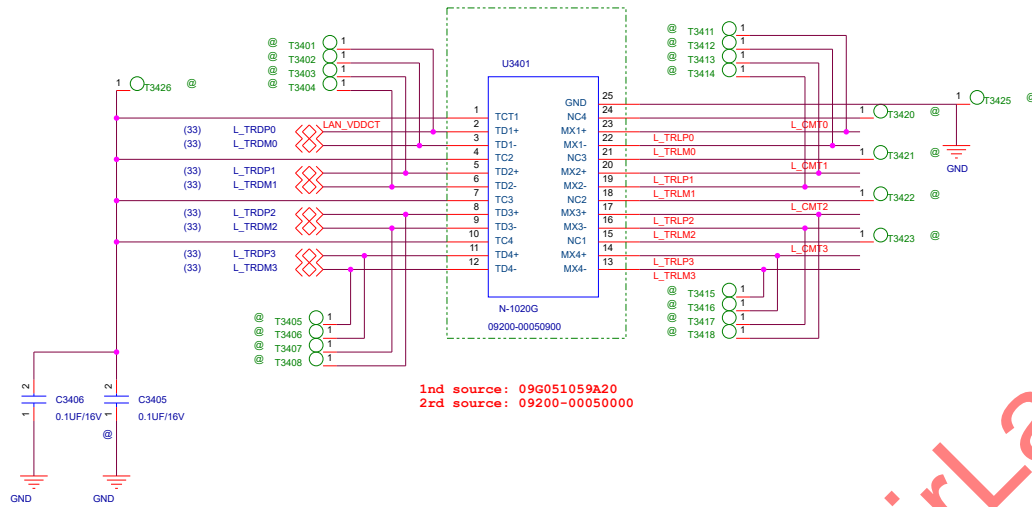


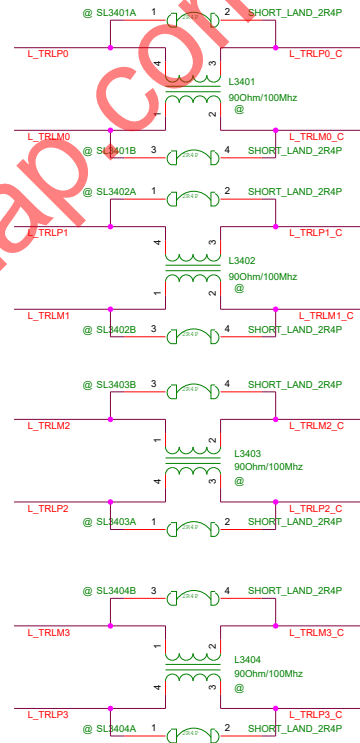
Table 17. Power Sequence Parameter					
Symbol	Description	Min	Typical	Max	Units
Rt1	3.3V Rise Time	0.5	-	100	ms
Rt2	3.3V Off Time	50	-	-	ms
Rt3	1.0V (REGOUT) Settle Time	-	-	15	ms

Note: See the following section for power sequence requirements.

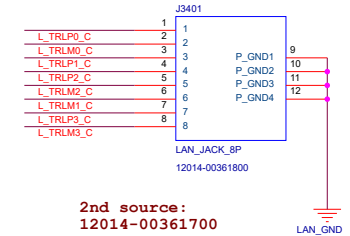
# RJ45 con.



R2.2 [Chip]  
Del R3401 for 非繞線式Transformer 1020G




TOP, In1, In2, In3, Bottom層需鋪LAN-Gnd



BOM

ASUS		Project Name	Rev
Title : LAN_AR8171_RJ45			R1.0
Size B	Dept.: ASUS/TEK COMPUTER INC.	Engineer: EE	
Date: Monday, January 04, 2016	Sheet 34	of 102	



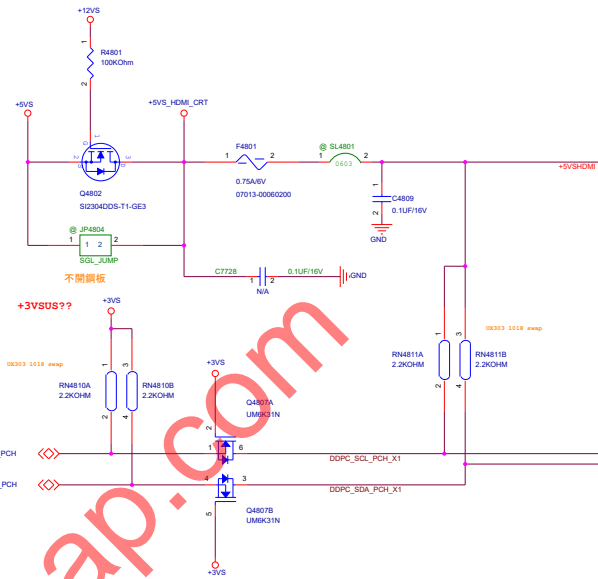
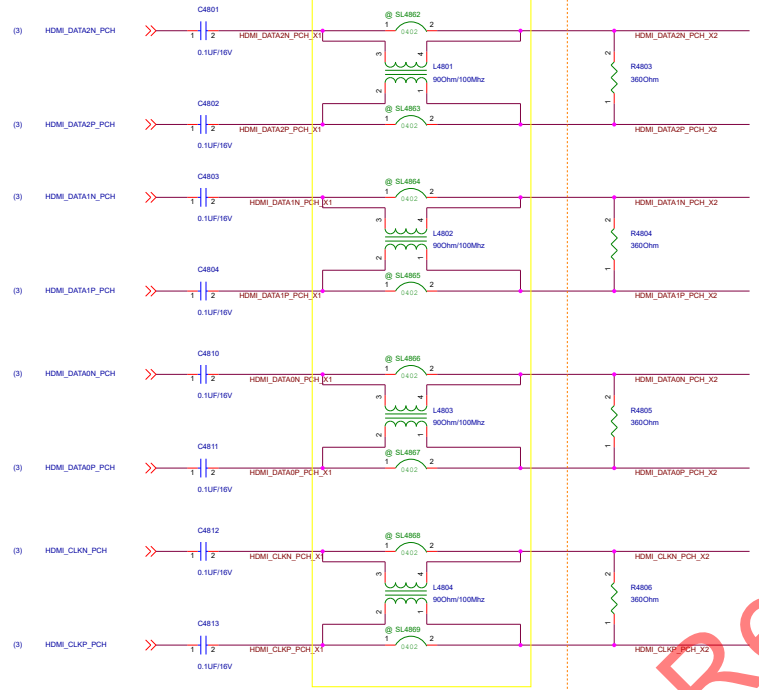
BOM		Project Name	Rev
REV		X456	R1.0
Title :		CPU_PCH_POEWR.GND	
Size	Dept.:	ASUSTek COMPUTER INC.	Engineer: EE
B			
Date:	Monday, January 04, 2016		Sheet 27 of 102

# HDMI type-D

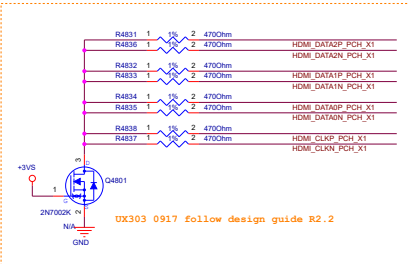
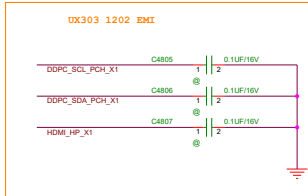
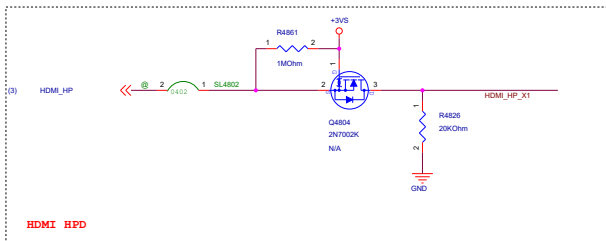
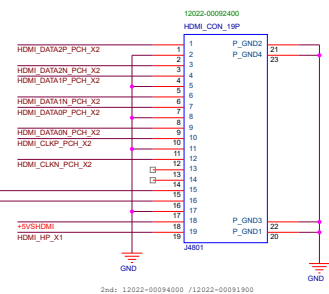
Close to CONNECTOR

Near CON J4801

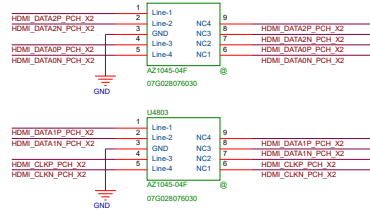
ER-022



HDMI CON.



UX303 1016 SWAP



BOM

ASUS		Project Name	Rev
X556UV			R1.0
Title : HDMI-type D			
Size	Dept.:	ASUSTek COMPUTER INC. Engineer:	EE
C			
Date: Monday, January 04, 2016		Sheet	48 of 102

C5002 put besides J5001.4

+5V

+5V

0V

GND

Remove diode(+5V to GND) for using 4-wires PWM FAN.

3V5

R5001 10kOhm

100pF/50V

100pF/50V

100pF/5V

J5001

4 5 6

3 4 SIDE2

2 3 SIDE1

1 2

WhB\_CON\_4P

12G17000004B

2nd source: 12G17000004V

(30) FAN0\_PWM

(30) FAN0\_TACH

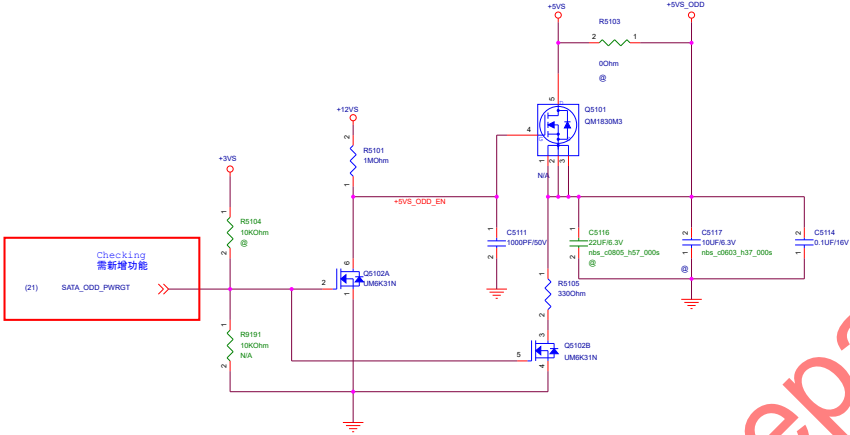
[illegible]

NCT7717U I2C/SMBus address is 1001000xb (x is R/W bit).

The default value could be set after power up 100ms by different pull-up resistor of ALERT# pin :

PULL-UP RESISTOR		TEMPERATURE (°C)
ALERT	2KΩ	75
	7.5KΩ	90
	10.5KΩ	100
	14KΩ	105
	18.7KΩ	110

# SATA ODD POWER



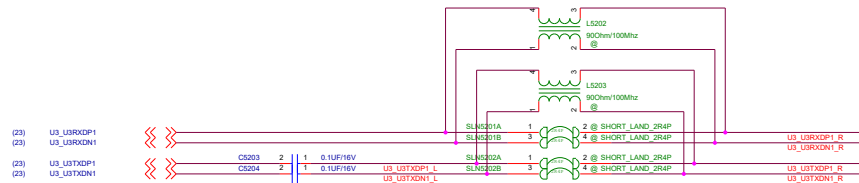
RepairLap.com

BOM

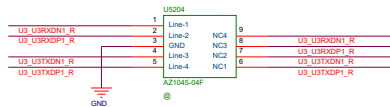
Project Name		Rev
ASUS X556UV		R1.0
Title : SATA HDD & ODD		
Size	Dept.: ASUSTek COMPUTER INC.	Engineer: EE
C	Date: Monday, January 04, 2016	Sheet 51 of 102

# USB 3.0 con.

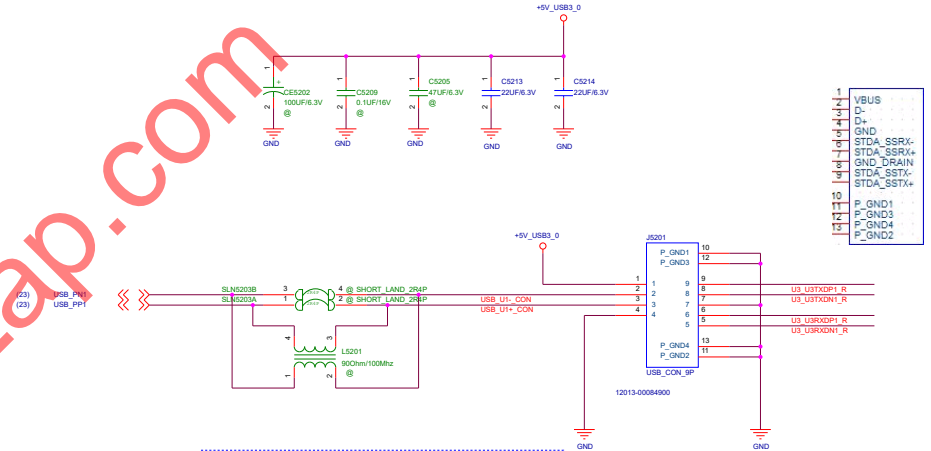
## USB3.0 Bus



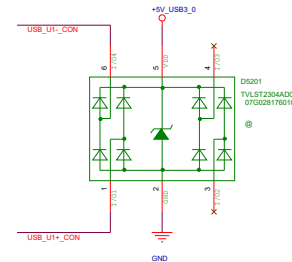
## USB3.0 ESD-Protection



## USB charge PORT



## USB2.0 ESD-Protection



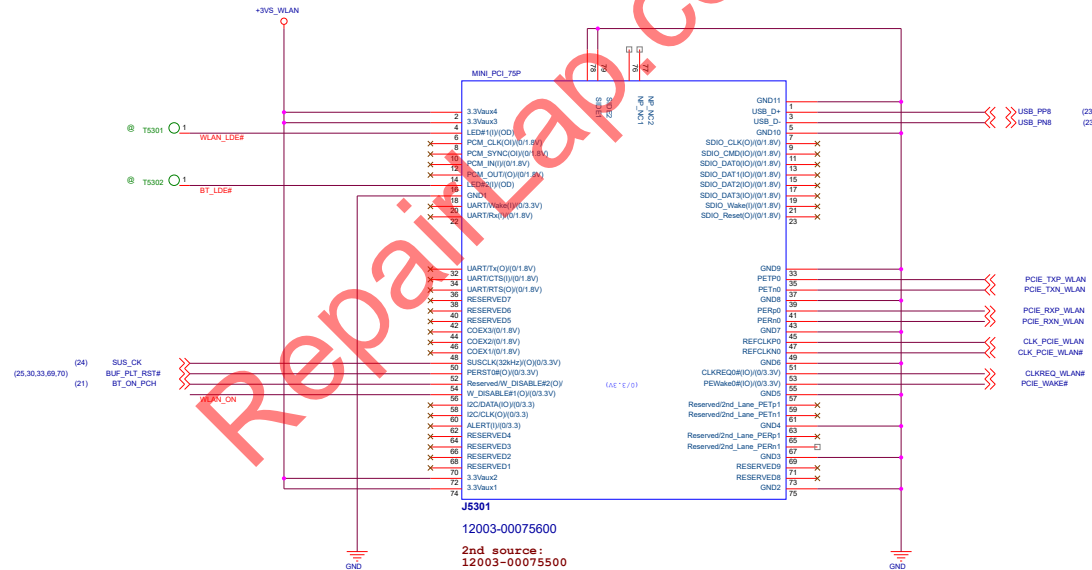
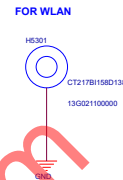
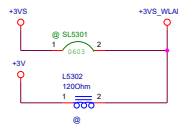
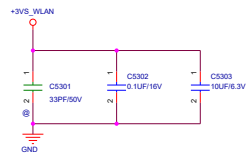
2nd source: 12013-00085100 / 12013-00084900

BOM

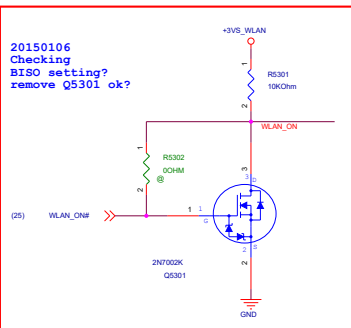
Project Name		Rev
ASUS X556UV		R1.0
Title : USB 3.0 + 2.0 CONN.		
Size	Dept.	Engineer
Custom	ASUSTek COMPUTER INC.	EE
Date: Monday, January 04, 2016	Sheet	52 of 102



# WLAN con.

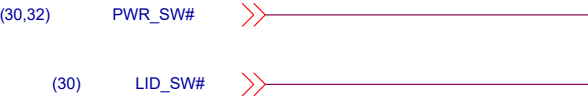


20150106  
Checking  
BISO setting?  
remove Q5301 ok?

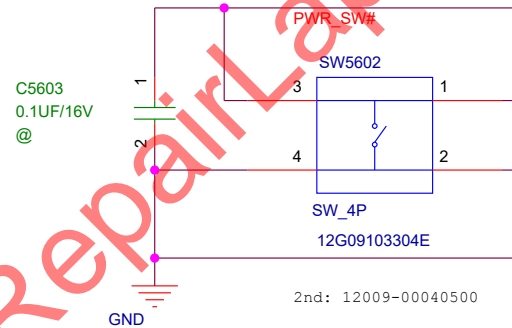
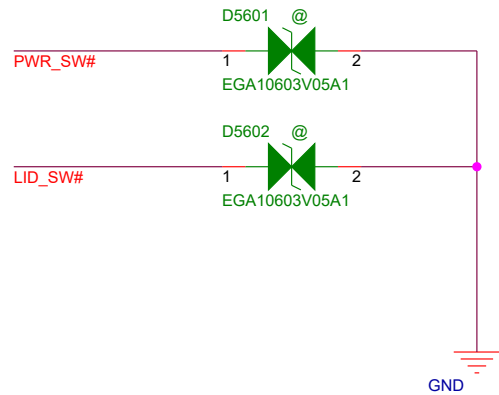
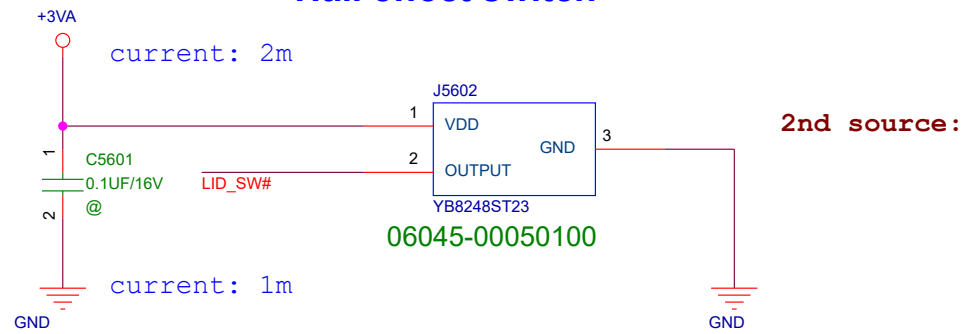


BOM


Project Name		Rev
ASUS X556UV		R1.0
Title : MINICARD(WLAN)		
Size	Dept.	Engineer
Custom	ASUSTek COMPUTER INC.	EE
Date: Monday, January 04, 2016	Sheet	53 of 102

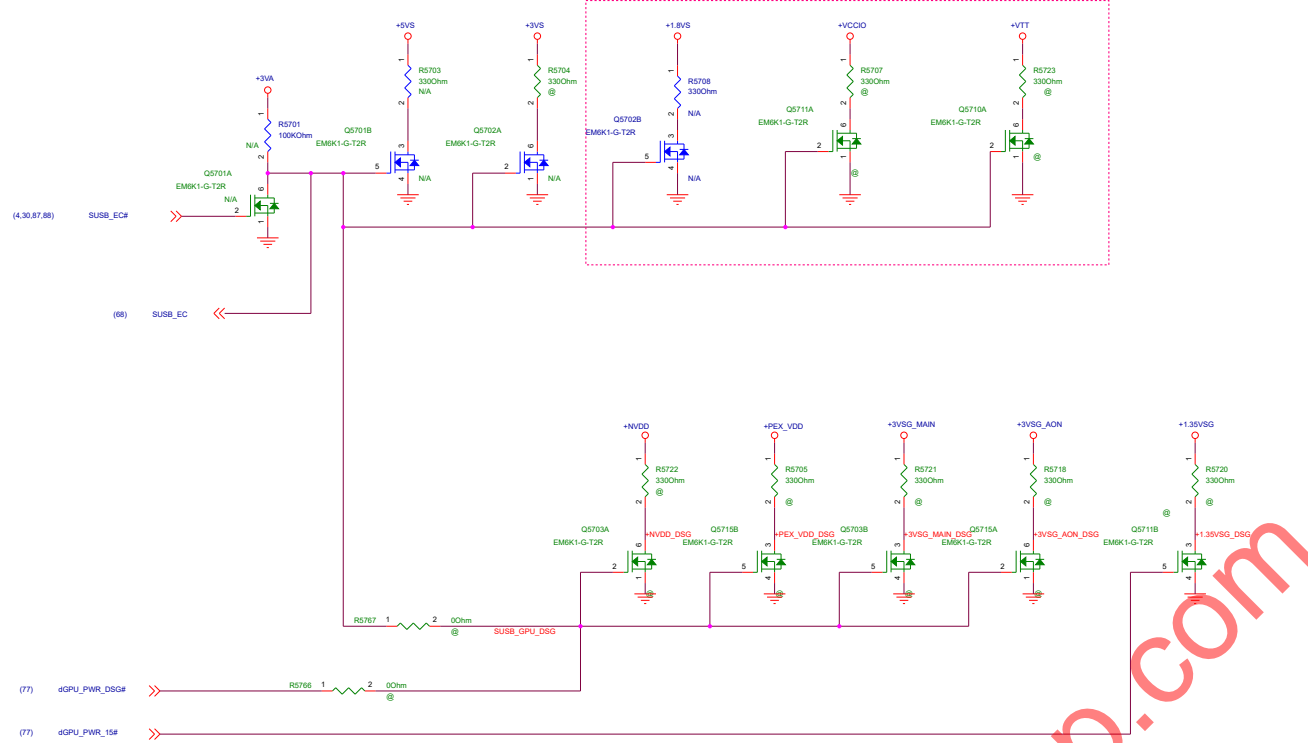


## Hall effect switch

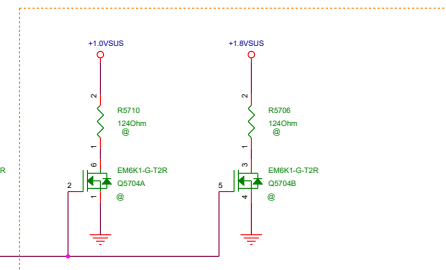
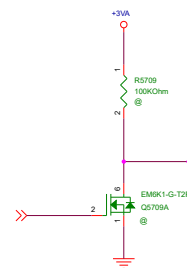
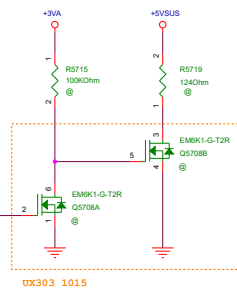
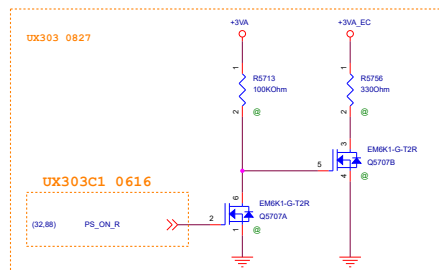
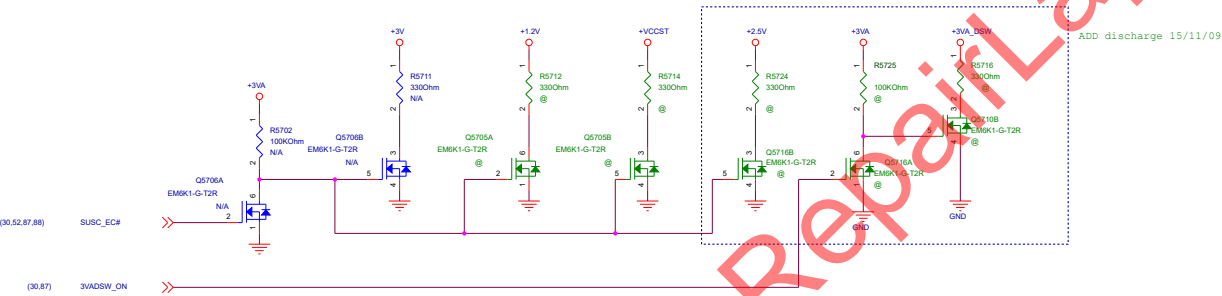


### BOM

		Project Name	Rev
		<b>X556UV</b>	R1.0
Title : <b>PWR_SW&amp;HALL_SW</b>			
Size A	Dept.: <b>ASUSTeK COMPUTER INC.</b> Engineer: <b>EE</b>		
Date: <b>Monday, January 04, 2016</b>	Sheet	<b>56</b>	of <b>102</b>

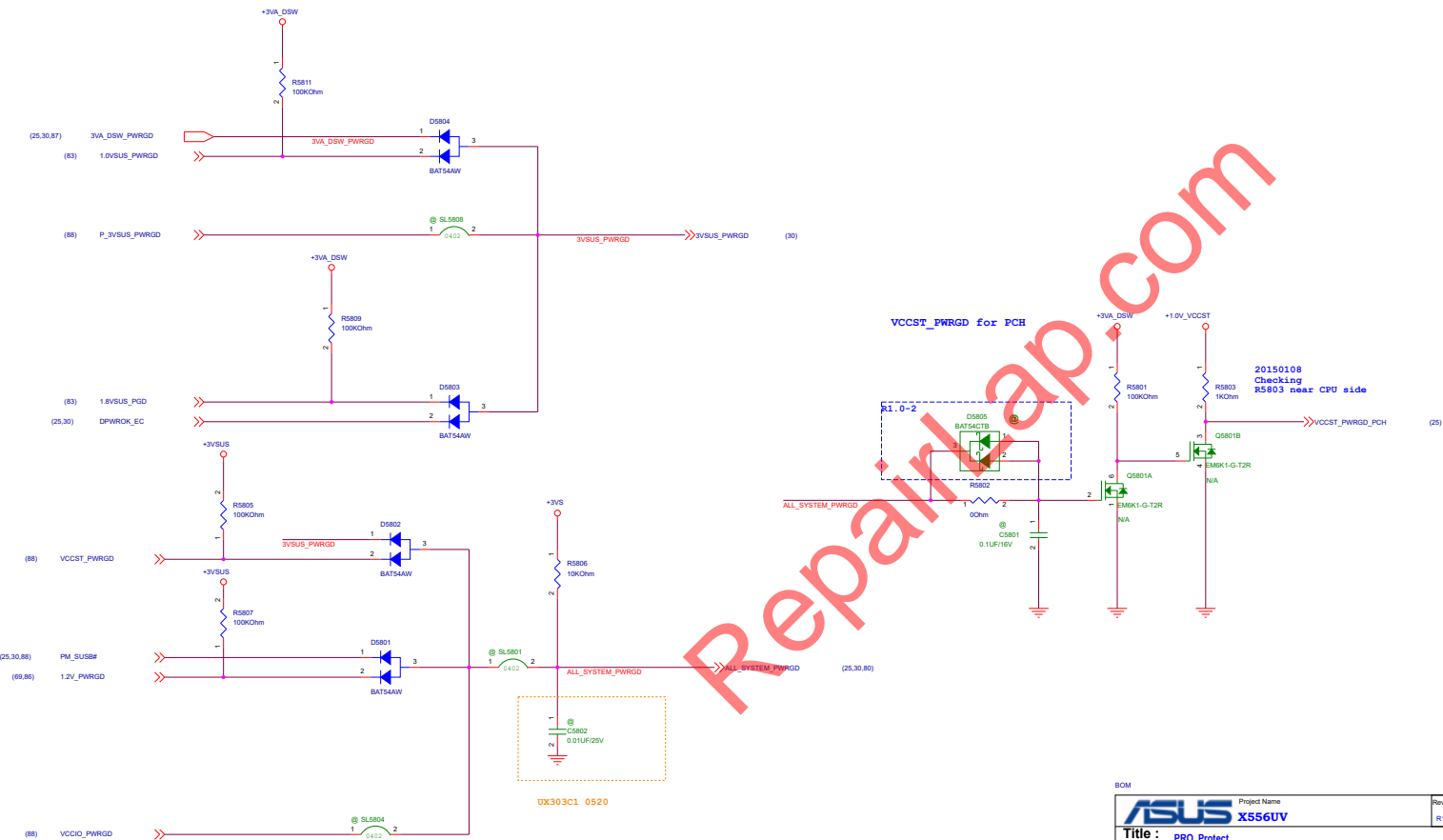


12/24 Stuff R5711 and R5708

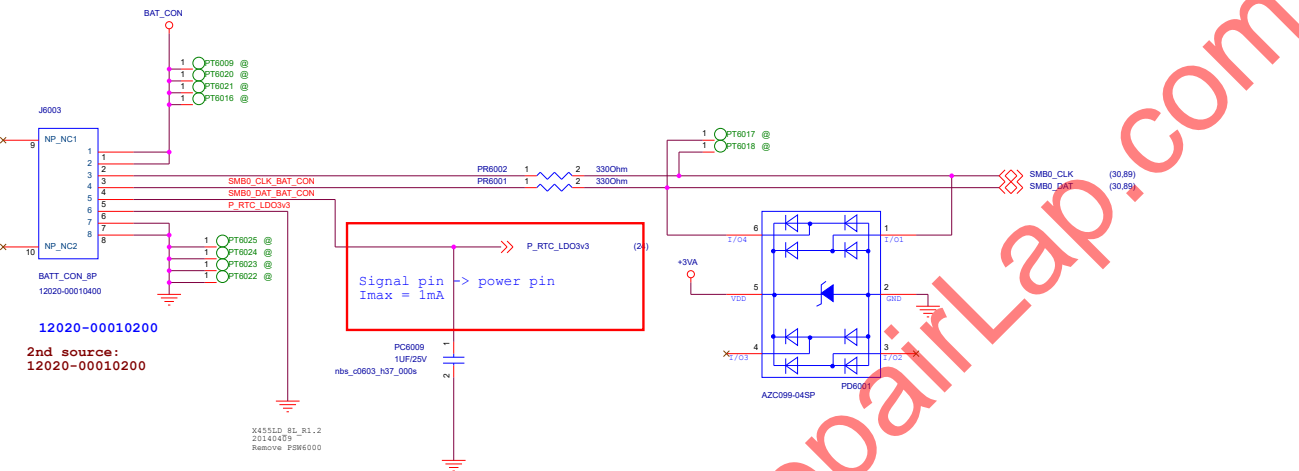



BOM

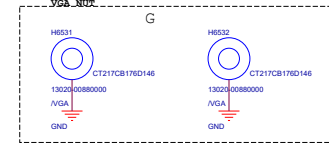
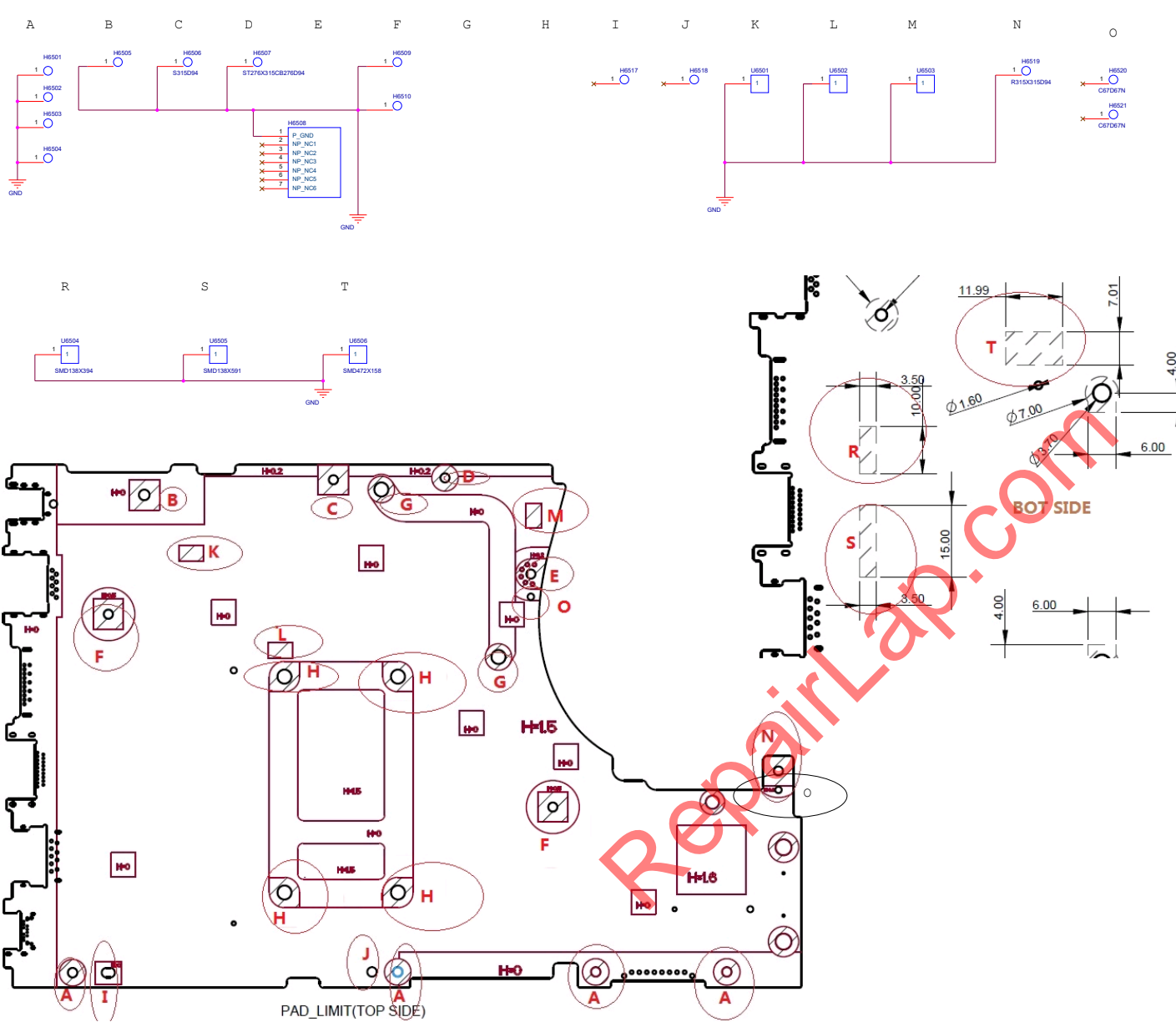
Project Name		Rev
ASUS X556UV		R1.0
Title : DSG_Discharge		
Size	Dept.: ASUStek COMPUTER INC.	Engineer: EE
C	Date: Monday, January 04, 2016	Sheet 57 of 102



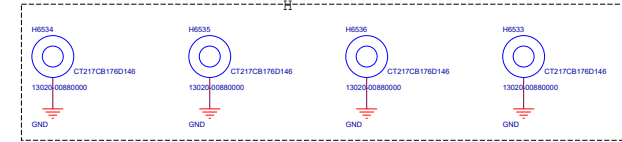
```
0603 Bead rule:
33W:Bead*2;
45W,65W : bead* 3;
90W,120W,150W:Bead*4;
180W,230W: bead*6
```



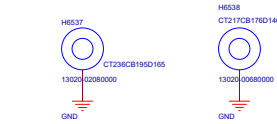
		Project Name <b>X556UV</b>		Rev <b>R1.0</b>	
<b>Title :</b> <b>DC &amp; BAT Connector</b>					
Size <b>A3</b>		<b>Dept.:</b> <b>ASUSTek COMPUTER INC. Engineer:</b>			
Date: <b>Monday, January 04, 2016</b>			Sheet <b>60</b> of <b>102</b>		



CPU\_NUT

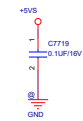
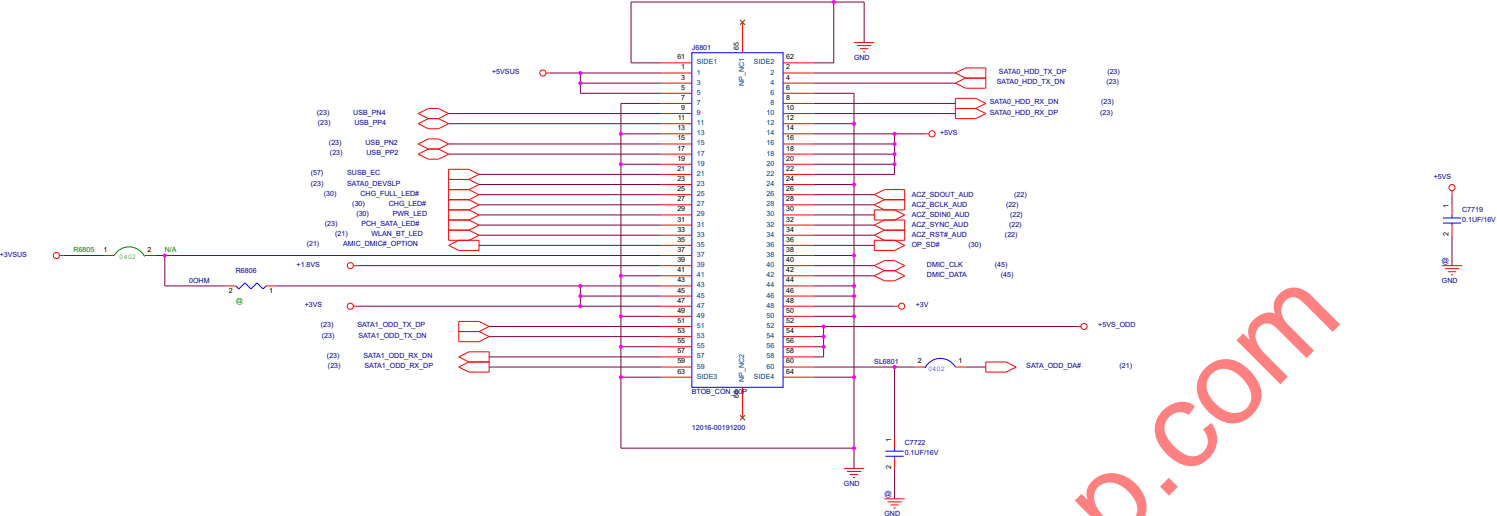


HDD\_BOARD\_NUT



BOM

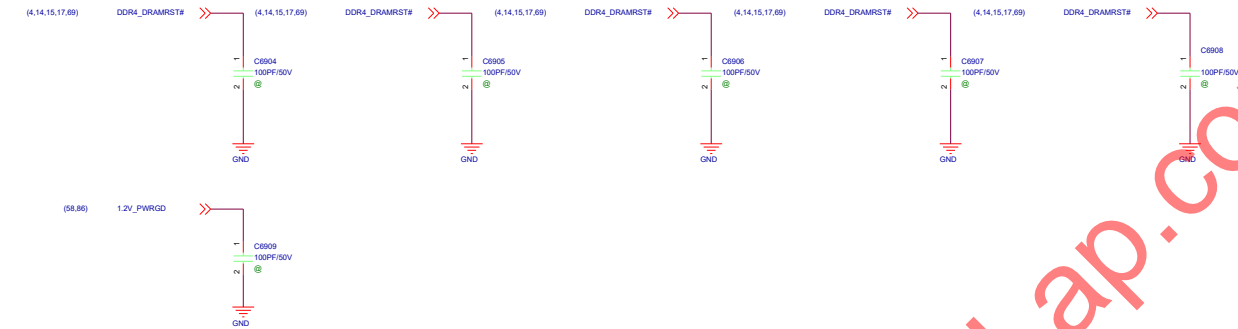
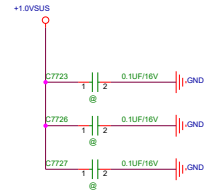
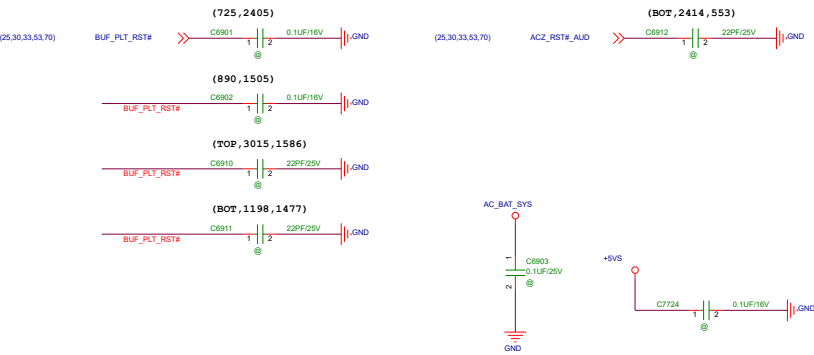
Project Name		Rev
ASUS		R1.0
Title : X556UV		
Size		
Dept.: ASUS&K COMPUTER INC. Engineer: EE		
Date: Monday, January 04, 2016		
Sheet		65 of 102



<Variant Name>

<b>ASUS</b>		Title : BT08	
ASUSTeK COMPUTER INC. NB3		Engineer: SZ/NB	
Size	Project Name		Rev
C	X556UV		R1.0
Date: Monday, January 04, 2016		Sheet	68 of 98

CAPS



RepairLap.com

BOM

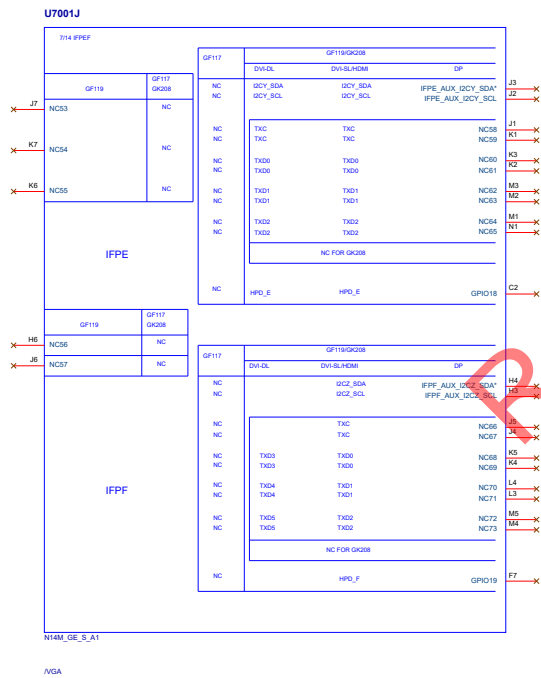
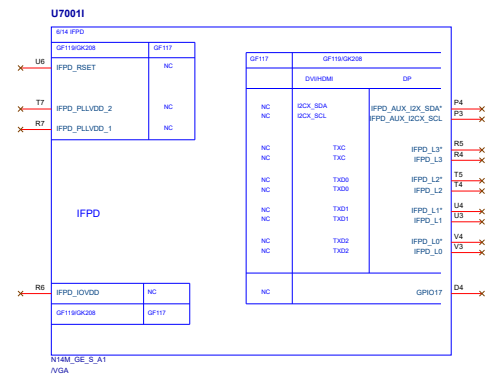
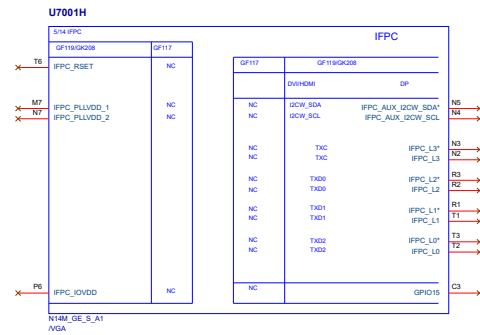
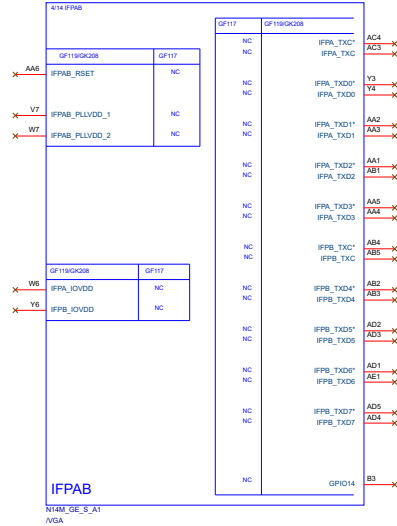
<b>ASUS</b>		Project Name	Rev
		<b>X556UV</b>	R1.0
Title : <b>EMI</b>			
Size	Dept.:	ASUSTek COMPUTER INC.	Engineer: <b>EE</b>
C			
Date: Monday, January 04, 2016		Sheet	69 of 102



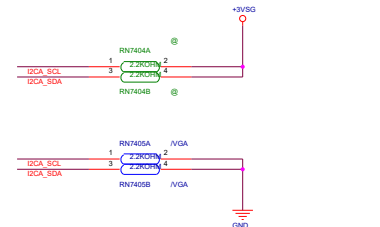
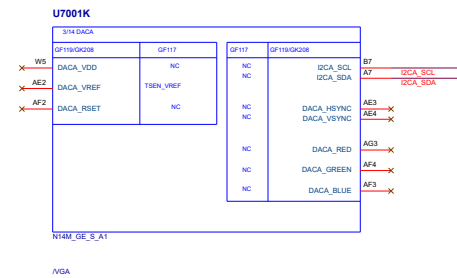




BCM



CRT





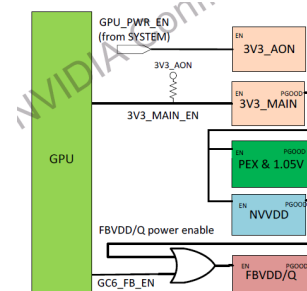
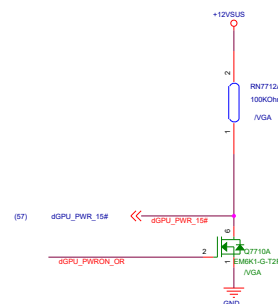
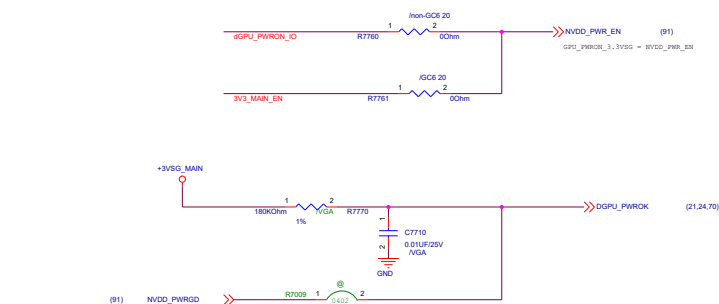
1G: 03007-00030300 SAMSUNG/K4W2G16460-BC1A 920:PD 45.3K 930/940: PU20K  
1G:03006-00080700 MICRON/MT41J128M16JF9-093G:K 920:PU 5K 930/940: PU15K  
2G: 03007-00021100 HYNIX/H5TC64CFR-NOC 920:PD 4.99K 930/940: PD 15K  
03007-00020900 MICRON/MT41J256M16HA-093G:E 920:PU 30.1K 930/940: PD 24.9K

N16V-GM-S

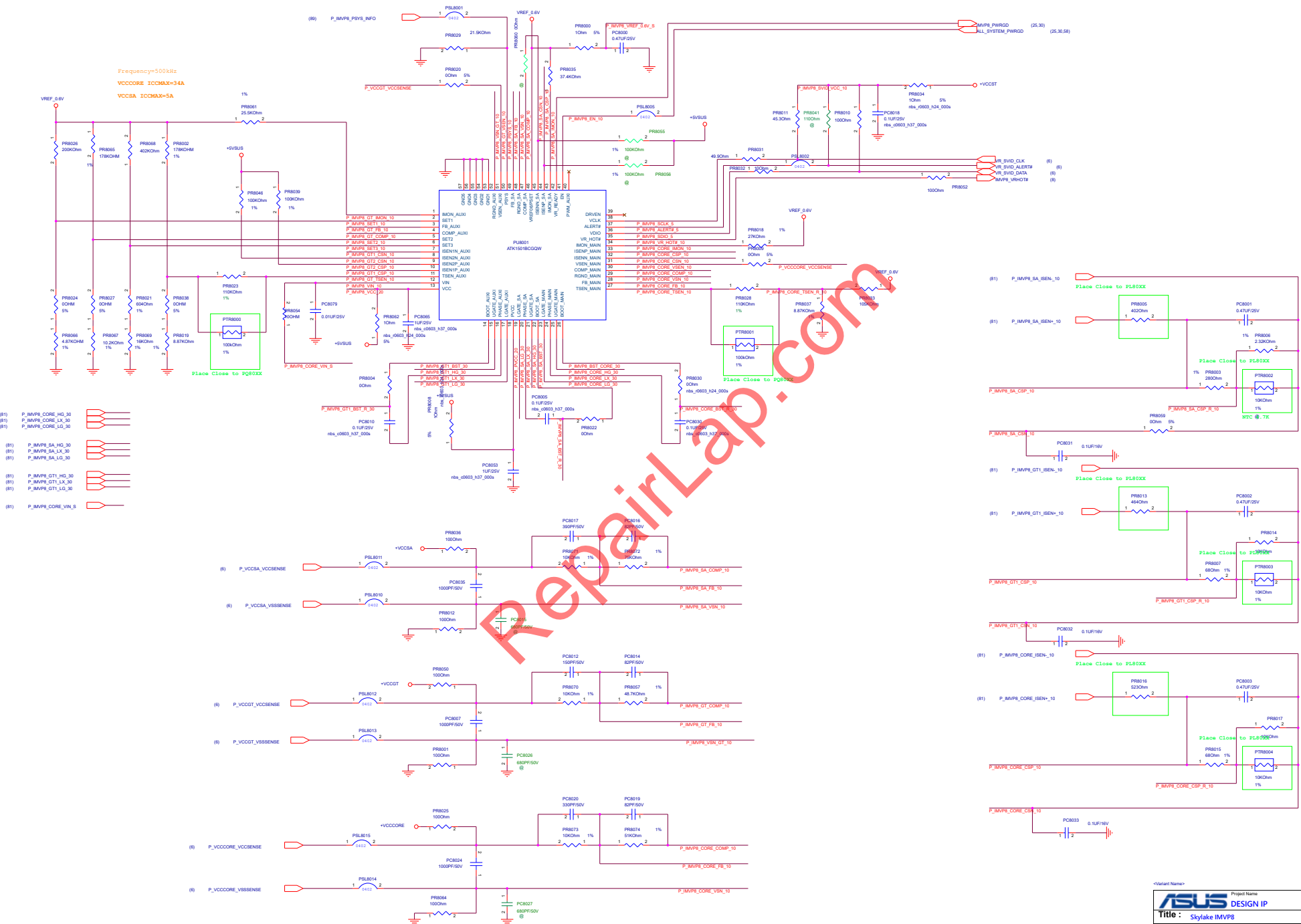




## dGPU Core Power Sequence

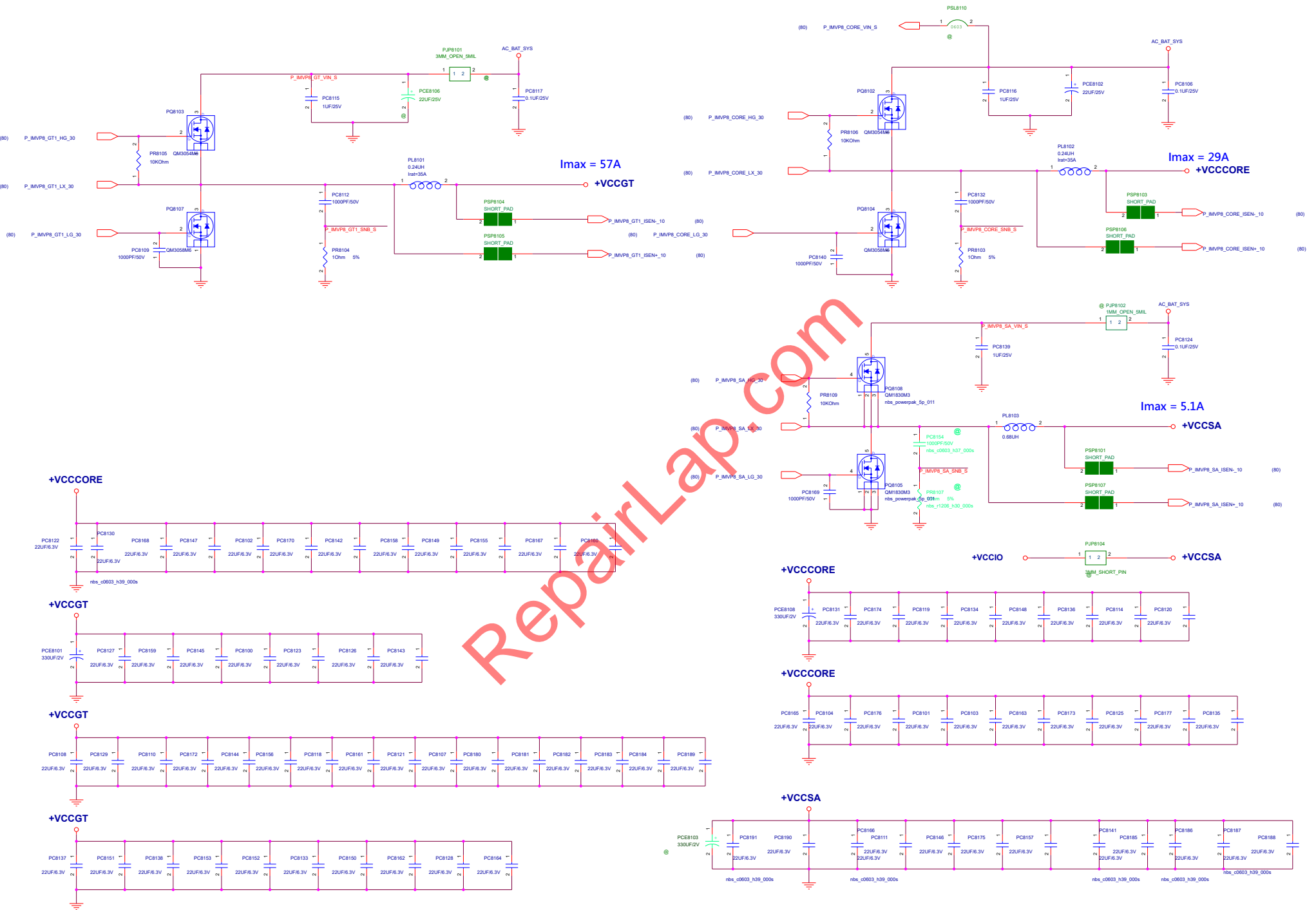


## Skylake IMVP8 Power [For CPU]



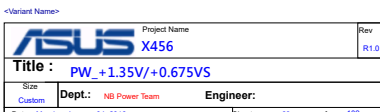


# Skylake IMVP8 Power (2) [For CPU]



<Variant Name>

State	Pin7(S3)	Pin8(S5)	VDDQ	VTTREF	VTT
S0	1	1	On	On	On
S3	0	1	On	On	OFF(Hi-Z)
S4/S5	0	0	OFF (Discharge)	OFF (Discharge)	OFF (Discharge)



S3 And S5 Truth Table

State	Pin7(S3)	Pin8(S5)	VDDQ	VTTREF	VTT
S0	1	1	On	On	On
S3	0	1	On	On	OFF(Hi-Z)
S4/S5	0	0	OFF (Discharge)	OFF (Discharge)	OFF (Discharge)

+1.2V/+VTT [For DDR4]

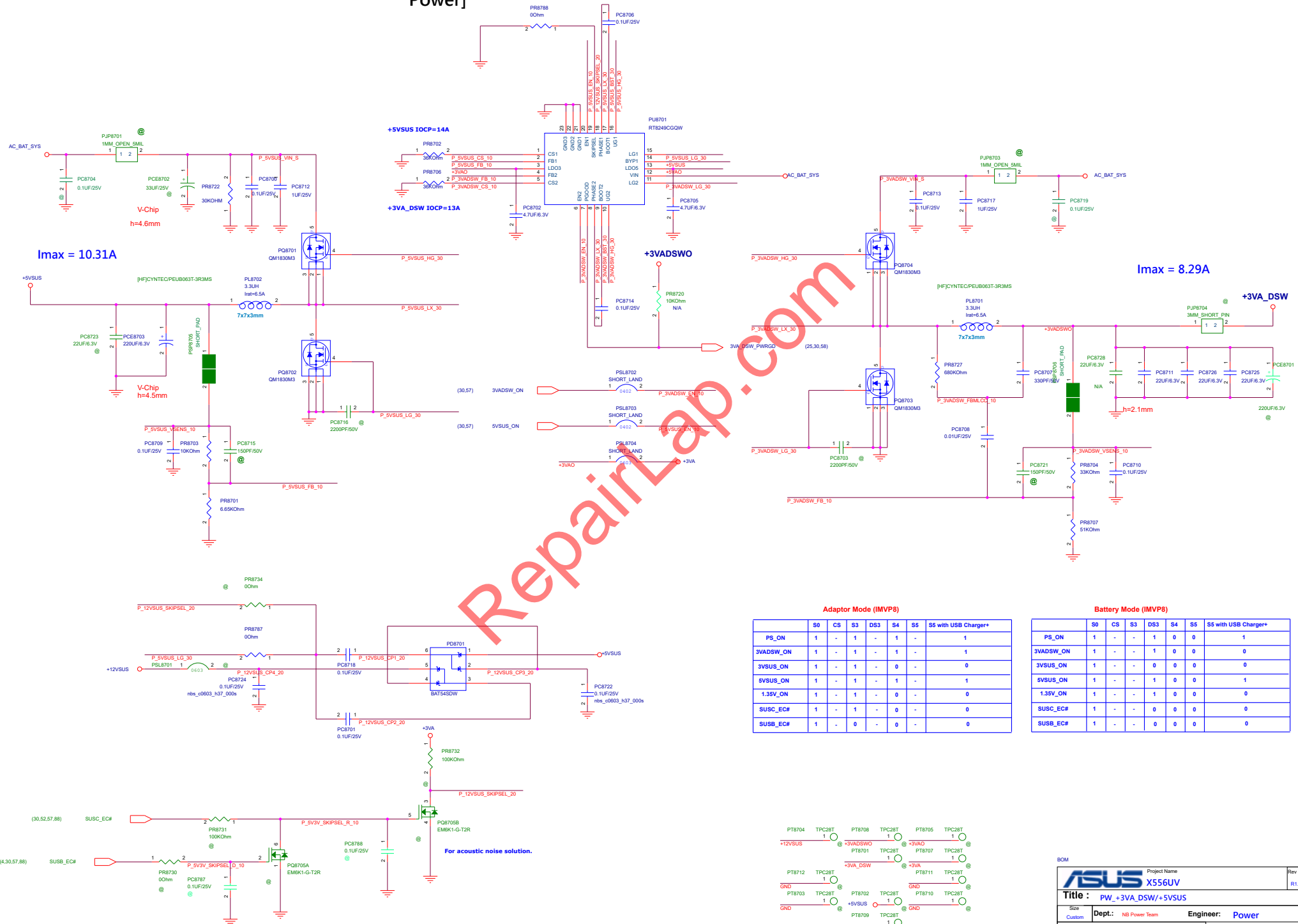
I<sub>max</sub> = 13A

OCp = ?A

UMA, With DGPU:改为Pure MLCC  
22uF/6.3V(0805), 壹四上三, 同時預留4.5mm  
V-Chip 330uF/2.5V不上件  
If:  
高度跟面積問題:改Pos-Cap ,100uF/2.5 or  
220uF/2V待討論

<Variant Name>

# +3VA DSW / +5VSUS [System Power]



BCM

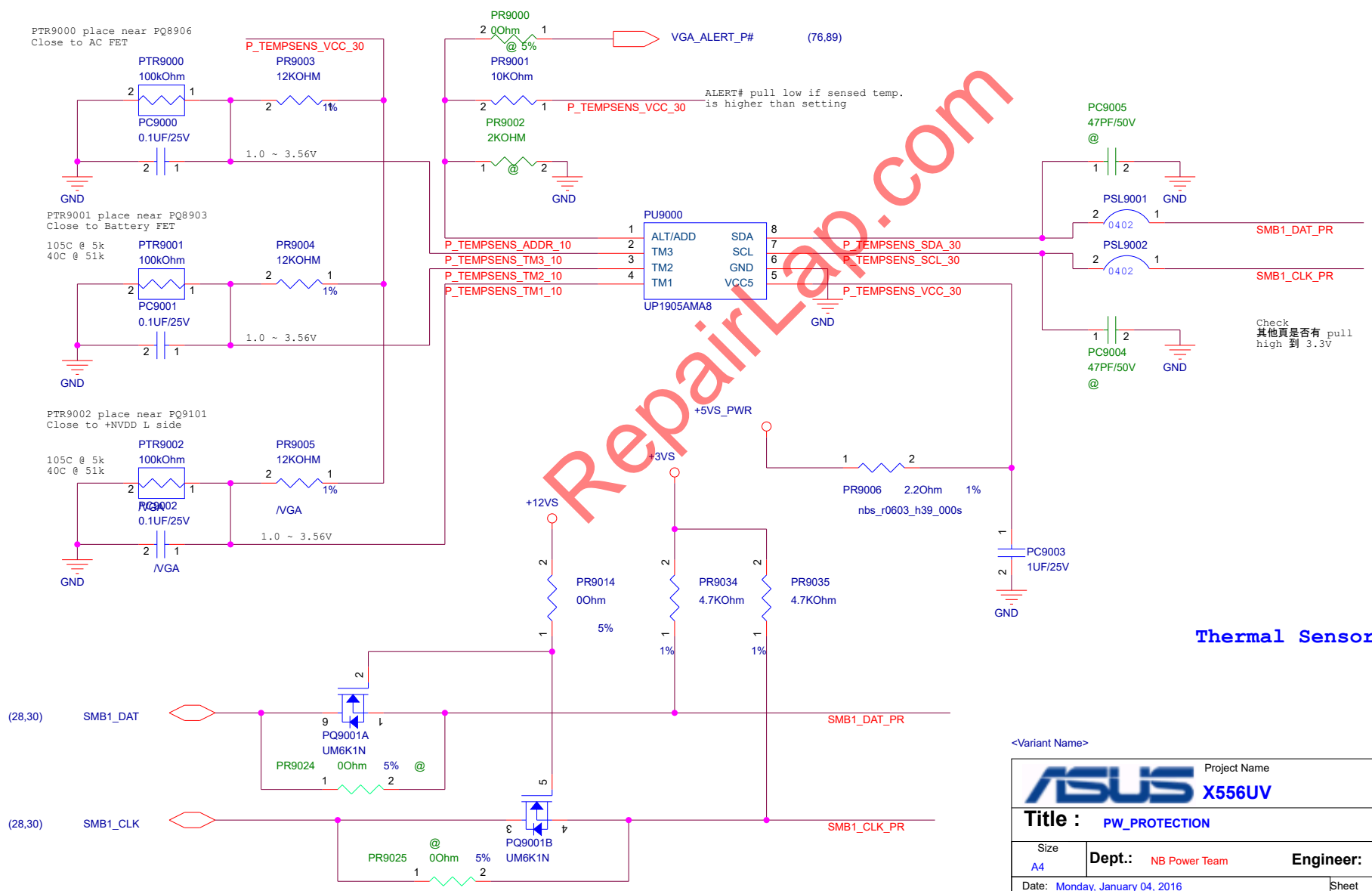


Address Selection Table

Address	0x7E	0x7C	0x7A	0x78	0x76	0x74	0x72	0x70
PR9001	10k	1.5k	2k	3.6k	3.9k	4.3k	5.1k	6k
PR9002	Open	8.2k	6.2k	6.8k	4.7k	3.6k	2.7k	2k

Register Address

Address	0x00	0x01	0x02	0x03	0x04	0x05	0x06
R/W	W	W	W	R	R	R	R
Function	Temp. alert threshold setting			Sensed temp. data		bit 4 = 0 bit 5 = 0 bit 6 = 0 When ALERT# assert	



Thermal Sensor

<Variant Name>



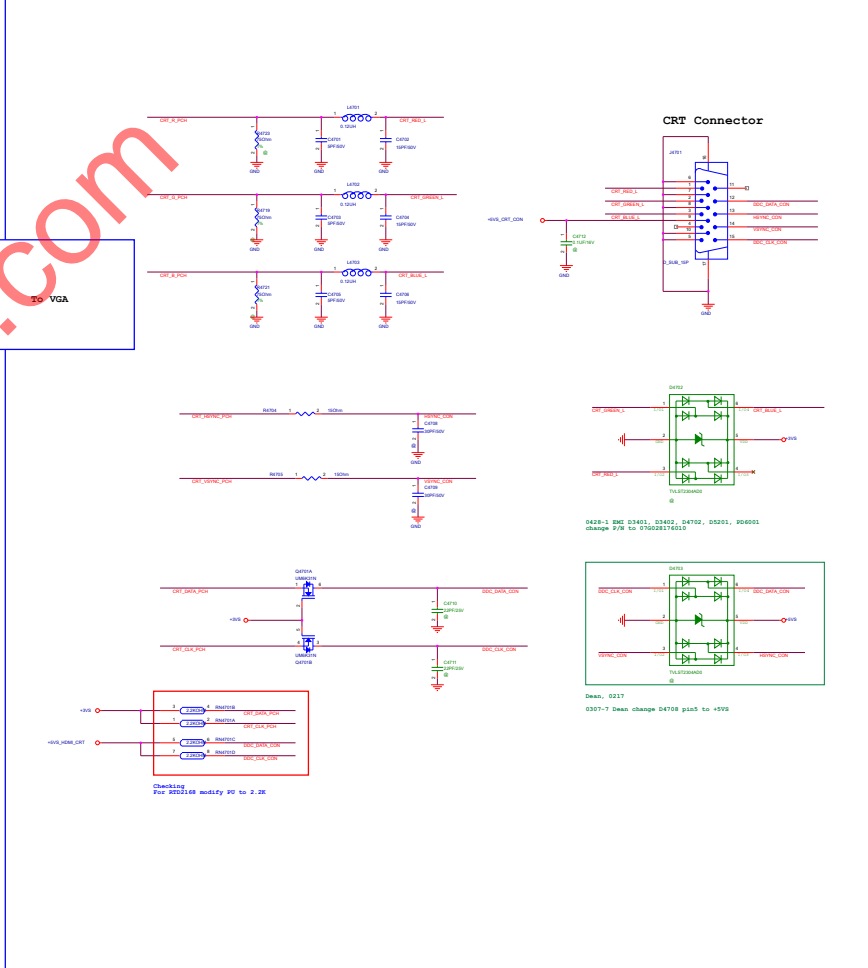
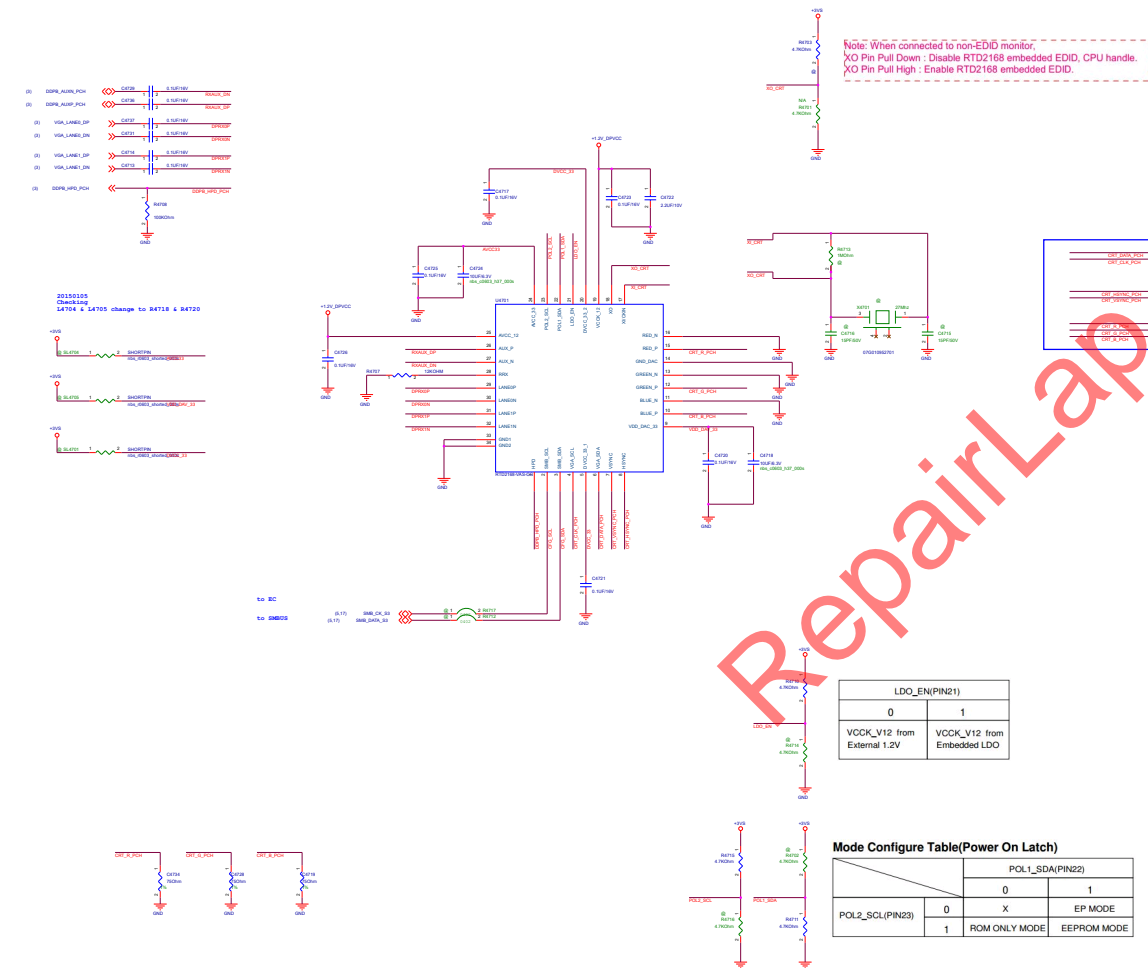






# EDP to VGA

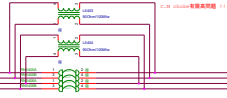
# CRT D-SUB



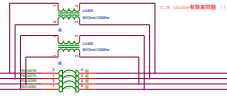
DPP CC Pull-Up Requirement for USB Type-C Power Options

USB Power	CC Pull-Up (1.5V to 3.3V)	CC Pull-Up (3.3V to 5V)
Default USB Power	50k Ohm $\pm 1\%$	30k Ohm $\pm 1\%$
1.5A @ 5V	22k Ohm $\pm 1\%$	12k Ohm $\pm 1\%$
3.0A @ 5V	10k Ohm $\pm 1\%$	4.7k Ohm $\pm 1\%$

USB3.0 Bus

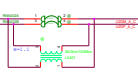


USB3.0 Bus



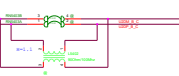
USB2.0

C.M. (Common Mode) 電壓差問題 (1)

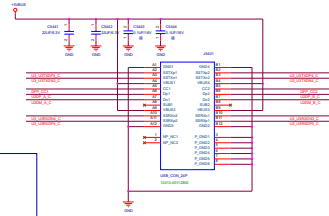
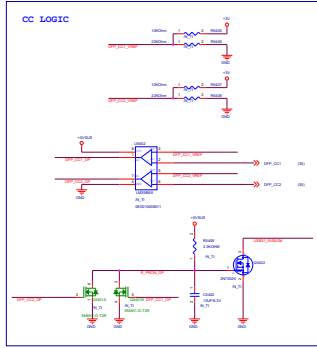


USB2.0

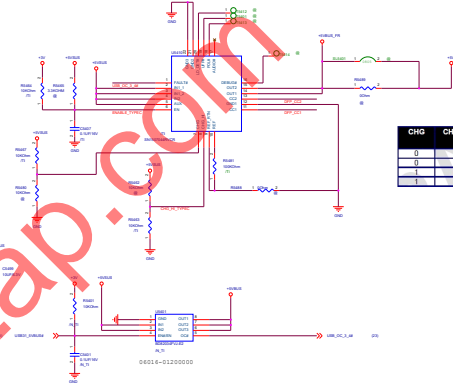
C.M. (Common Mode) 電壓差問題 (1)



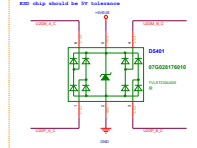
CC LOGIC



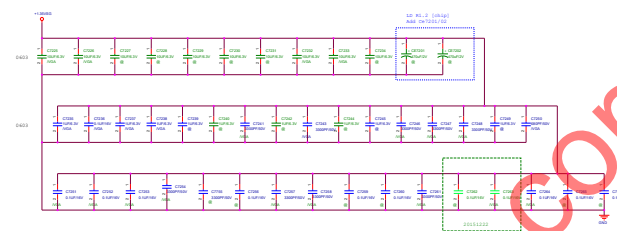
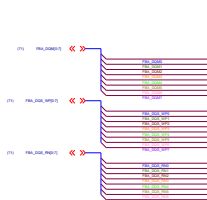
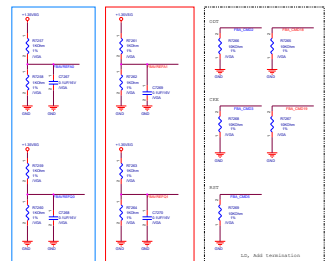
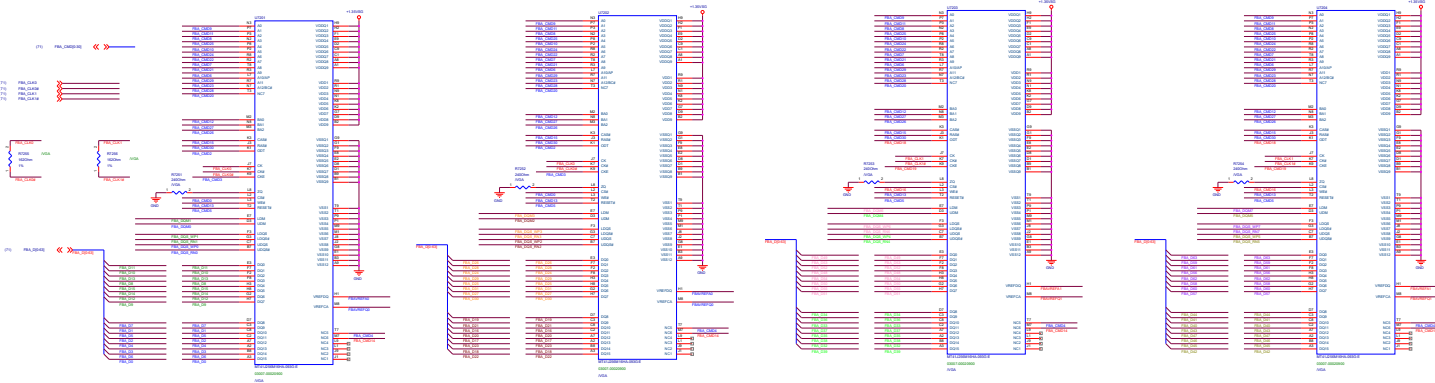
USB3\_Port\_Power\_Switch



USB2.0 ESD-Protection

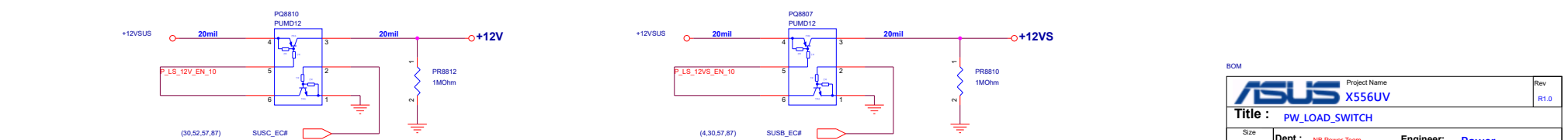
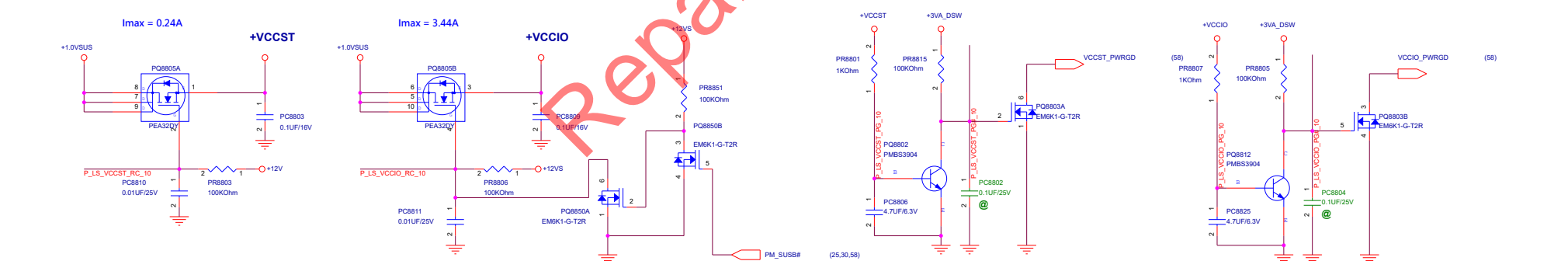
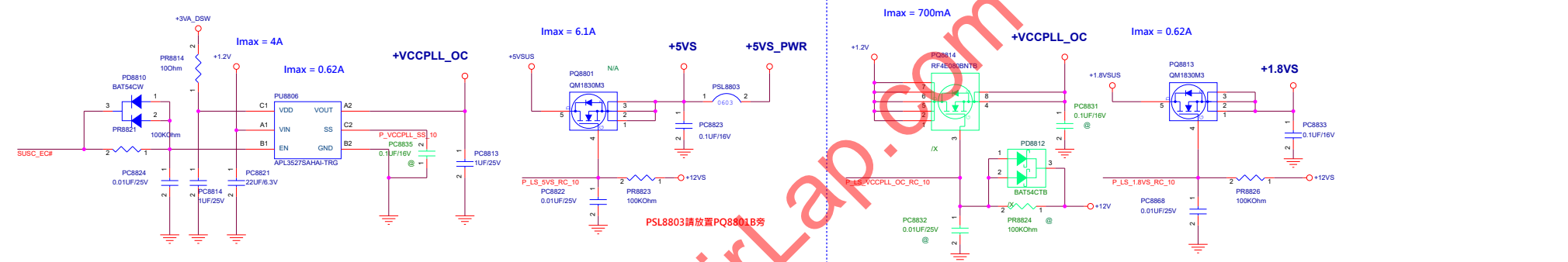
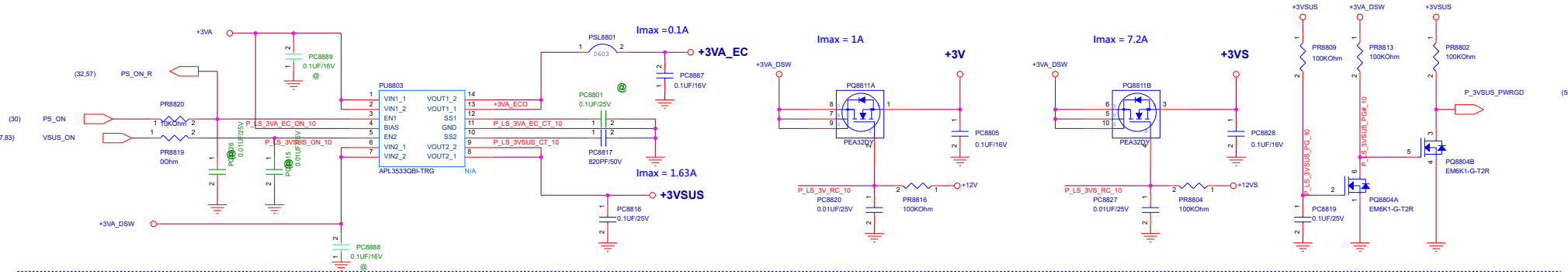


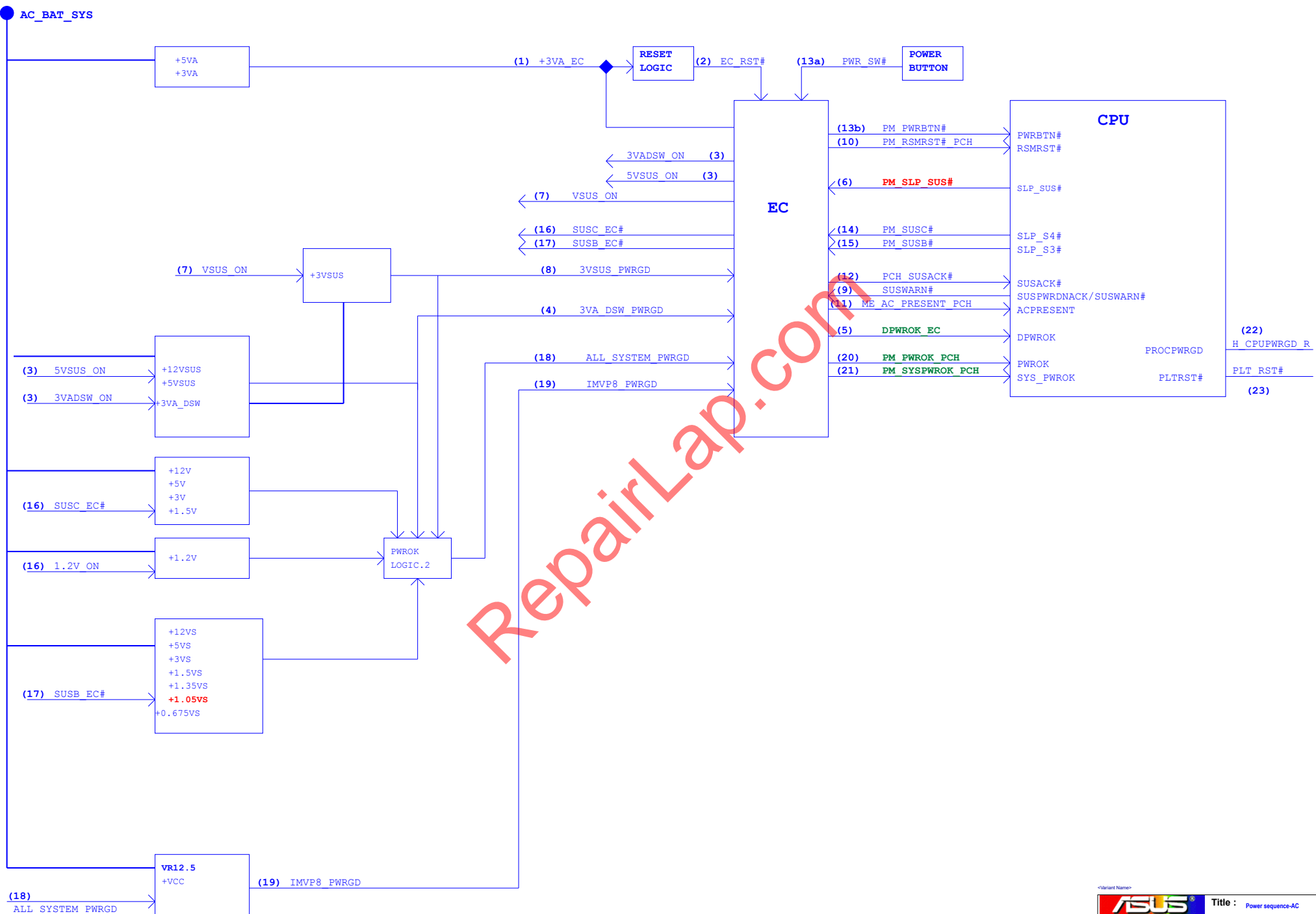
CHG	CHG_HI	CC Capability Broadcast	Current Limit	Load Detect Threshold
0	0	STD	0.7 A	NA
0	1	STD	1.0 A	NA
1	0	1.5 A	1.0 A	NA
1	1	3.0 A	3.0 A	1.77 A



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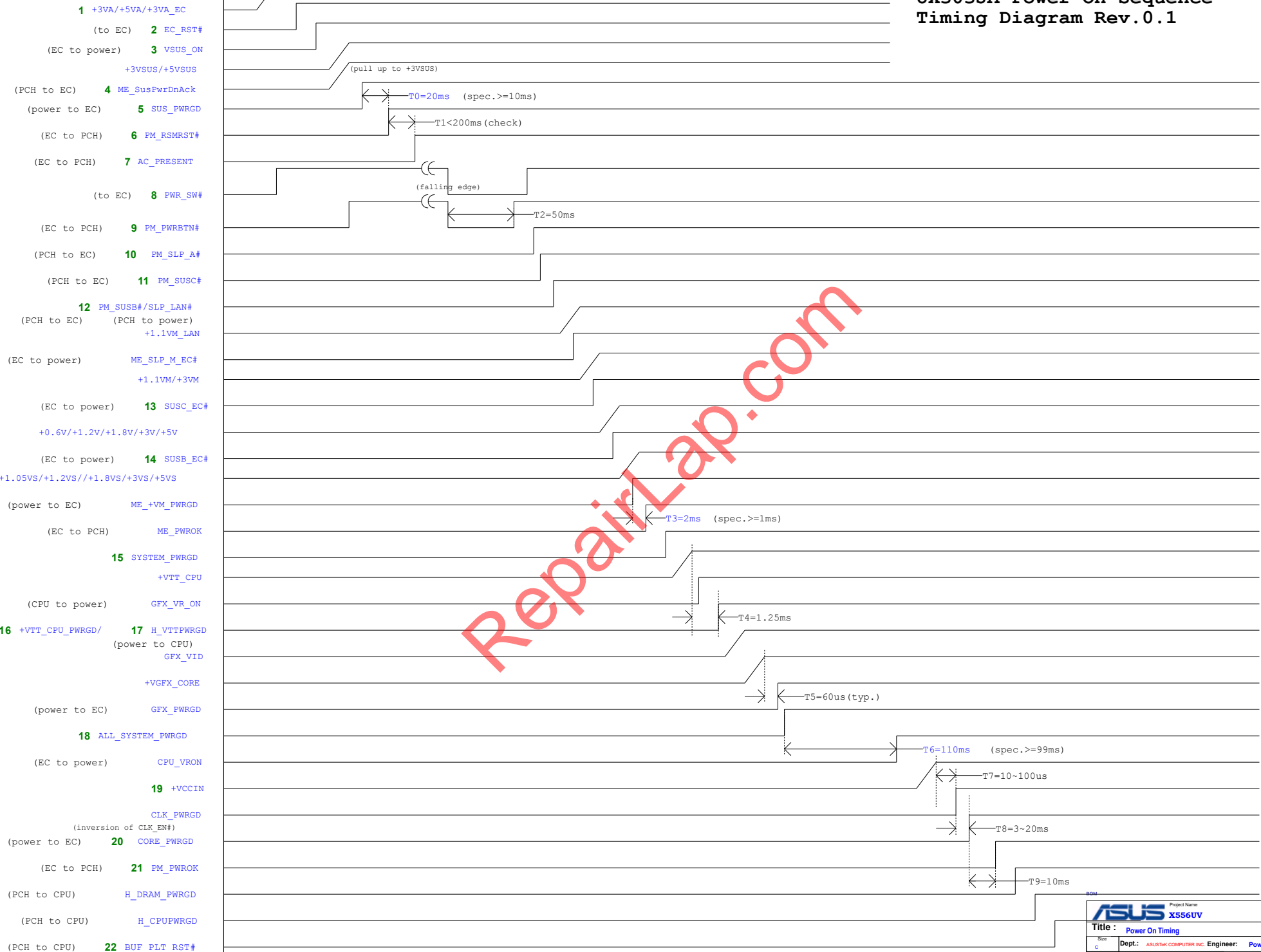
# Load Switch



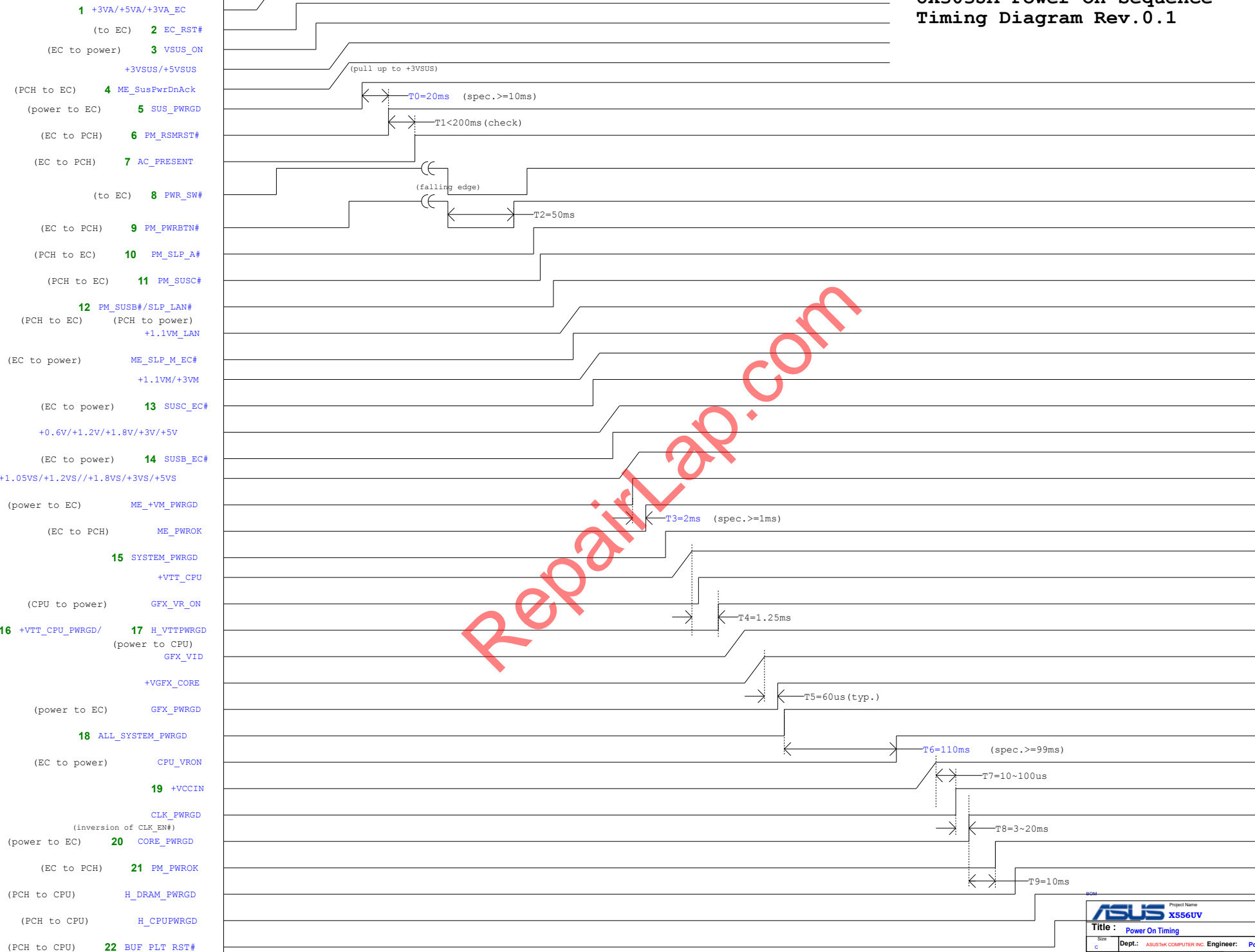



&lt;Variant Name&gt;










		Project Name	Rev
		<b>X556UV</b>	1.0
Title : DIM_DDR3 SO-DIMM A0			
Size Custom	Dept.:	Engineer:	<b>SZ/EE</b>
Date: Monday, January 04, 2016	Sheet	16	of 102

BOM

		Project Name <b>X556UV</b>		Rev <b>R1.0</b>
Title : <b>NGFF_WWAN</b>				
Size <b>C</b>	Dept.: <b>ASUSTeK COMPUTER INC.</b>		Engineer: <b>EE</b>	
Date: <b>Monday, January 04, 2016</b>			Sheet <b>59</b>	of <b>102</b>

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BOM

		Project Name	Rev
		X556UV	R1.0
Title : LVDS CONNECTOR			
Size	Dept.: ASUSTek COMPUTER INC. Engineer: EE		
C			
Date: Monday, January 04, 2016	Sheet	46	of 102

X556UJ SKU TABLE

ROM	GPU	RAM	SSD/1.1
60880970-H61630	/GPU	/RAM	/ADM1142
60880970-H61810	/GPU	/RAM	/ADM1142
60880970-H61811	/GPU	/RAM	/ADM1142


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ROM

		Project Name		Rev
		<b>X556UV</b>		R1.0
Title : <b>System Setting</b>				
Size	Dept.:	ASUSTek COMPUTER INC.		Engineer: EE
Date: Monday, January 04, 2016				1/4

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BOM

		Project Name	Rev
Title : CPU_XDP		X556UV	R1.0
Size	Dept.: ASUSTek COMPUTER INC. Engineer: EE		
C	Date: Monday, January 04, 2016 Sheet 7 of 102		



Project Name

**X556UV**

Rev

**R1.0**

**Title :** **PW\_+VCCPRIM\_CORE**

Size


**A3**

**Dept.:** **NB Power Team**


**Engineer:** **Power**


Date: **Monday, January 04, 2016**


Sheet **84** of **102**


		Project Name		Rev
		<b>X556UV</b>		R1.0
<b>Title :</b> <b>POWER_+VGFX_CORE</b>				
Size Custom	<b>Dept.:</b> NB Power Team		<b>Engineer:</b>	<b>Power</b>
Date:   Monday, January 04, 2016			Sheet	85     of     102





		Project Name		Rev
		<b>X556UV</b>		0.9
<b>Title :</b> <b>POWER_+VGFX_CORE</b>				
Size Custom	<b>Dept.:</b> <b>ASUSTeK COMPUTER INC.</b> <b>Engineer:</b> <b>EE</b>			
Date: <b>Monday, January 04, 2016</b>			Sheet	94     of     102


		Project Name		Rev
		X556UV		0.9
Title : POWER_+VGFX_CORE				
Size Custom	Dept.: ASUSTeK COMPUTER INC. Engineer: EE			
Date: Monday, January 04, 2016			Sheet	95 of 102


		Project Name <b>X556UV</b>		Rev <b>0.9</b>
<b>Title :</b> <b>POWER_+VGFX_CORE</b>				
Size <b>Custom</b>	<b>Dept.:</b> <b>ASUSTeK COMPUTER INC.</b> <b>Engineer:</b> <b>EE</b>			
Date: <b>Monday, January 04, 2016</b>			Sheet <b>96</b>	of <b>102</b>

		Project Name		Rev
		X556UV		0.9
Title : POWER_+VGFX_CORE				
Size Custom	Dept.: ASUSTeK COMPUTER INC. Engineer: EE			
Date: Monday, January 04, 2016			Sheet	92 of 102

		Project Name		Rev
		X456		R1.0
Title : PW_SKYLAKE-U (3)				
Size Custom	Dept.: NB Power Team		Engineer:	Power
Date: Monday, January 04, 2016			Sheet	82 of 102

		Project Name <b>X556UV</b>		Rev <b>0.9</b>
<b>Title :</b> <b>POWER_+VGFX_CORE</b>				
Size <b>Custom</b>	<b>Dept.:</b> <b>ASUSTeK COMPUTER INC.</b> <b>Engineer:</b> <b>EE</b>			
Date: <b>Monday, January 04, 2016</b>			Sheet <b>97</b>	of <b>102</b>

		Project Name		Rev
		X556UV		0.9
Title : POWER_+VGFX_CORE				
Size Custom	Dept.: ASUSTeK COMPUTER INC. Engineer: EE			
Date: Monday, January 04, 2016			Sheet	98 of 102

		Project Name		Rev
		<b>X556UV</b>		R1.0
<b>Title :</b> <b>small board_USB Port</b>				
Size	<b>Dept.:</b> <b>ASUSTeK COMPUTER INC.</b> <b>Engineer:</b> <b>SZ/EE</b>			
D				
Date: <b>Monday, January 04, 2016</b>			Sheet	11      of      102



<Variant Name>

Title

<Title>

Size

A

Document Number

<Doc>

Rev

<RevCode>

Date:


Monday, January 04, 2016


Sheet


19


of


102


		Project Name		Rev
		<b>X556UV</b>		R1.0
<b>Title :</b> <b>PCH-XDP</b>				
Size B	<b>Dept.:</b> <b>ASUSTeK COMPUTER INC.</b> <b>Engineer:</b> <b>EE</b>			
Date: <b>Monday, January 04, 2016</b>			Sheet <b>29</b>	of <b>102</b>


		Project Name		Rev
		<b>X556UV</b>		R1.0
<b>Title :</b> <b>small board_Screw_hole</b>				
Size	<b>Dept.:</b> <b>ASUSTeK COMPUTER INC.</b> <b>Engineer:</b>			
C				
Date:    Monday, January 04, 2016			Sheet	12      of      102

		Project Name		Rev
		<b>X556UV</b>		R1.0
<b>Title :</b> <b>CB-****</b>				
Size	<b>Dept.:</b> <b>ASUSTeK COMPUTER INC.</b> <b>Engineer:</b> <b>EE</b>			
C				
Date: <b>Monday, January 04, 2016</b>			Sheet	43      of      102


		Project Name		Rev
		<b>X556UV</b>		R1.0
<b>Title :</b> <b>AUD-SPEAKER CONN.</b>				
Size	<b>Dept.:</b> <b>ASUSTeK COMPUTER INC.</b> <b>Engineer:</b> <b>EE</b>			
A				
Date: <b>Monday, January 04, 2016</b>			Sheet	39      of      102


		Project Name		Rev
		<b>X556UV</b>		R1.0
<b>Title :</b> <b>AUD SPK-R CONN</b>				
Size  C	<b>Dept.:</b> <b>ASUSTeK COMPUTER INC.</b> <b>Engineer:</b> <b>EE</b>			
Date: <b>Monday, January 04, 2016</b>			Sheet	38                      of                      102


		Project Name		Rev
		<b>X556UV</b>		R1.0
<b>Title :</b> <b>TV_****</b>				
Size				
<b>C</b>	<b>Dept.:</b>	<b>ASUSTeK COMPUTER INC.</b>	<b>Engineer:</b>	<b>EE</b>
Date: <b>Monday, January 04, 2016</b>			Sheet	<b>49</b> of <b>102</b>


		Project Name		Rev
		<b>X556UV</b>		R1.0
<b>Title :</b> <b>SERIAL PORT</b>				
Size Custom	<b>Dept.:</b> ASUSTeK COMPUTER INC. <b>Engineer:</b> <b>EE</b>			
Date:   Monday, January 04, 2016			Sheet	35       of       102





		Project Name		Rev
		<b>X556UV</b>		R1.0
<b>Title :</b> <b>AUDIO_CX20752_Rev0.11_1</b>				
Size				
<b>A</b>	<b>Dept.:</b>	<b>ASUSTeK COMPUTER INC.</b>	<b>Engineer:</b>	<b>EE</b>
Date: <b>Monday, January 04, 2016</b>			Sheet	<b>36</b> of <b>102</b>


		Project Name		Rev
		<b>X456</b>		R1.0
Title : <b>AUD-****</b>				
Size	Dept.: <b>ASUSTeK COMPUTER INC.</b> Engineer: <b>EE</b>			
<b>C</b>				
Date: <b>Monday, January 04, 2016</b>			Sheet	<b>37</b> of <b>102</b>


		Project Name		Rev
		<b>X556UV</b>		R1.0
<b>Title :</b> <b>BD_USB2.0 x2_PHONE JACK</b>				
Size	<b>Dept.:</b> <b>ASUSTeK COMPUTER INC.</b> <b>Engineer:</b> <b>EE</b>			
A				
Date: <b>Monday, January 04, 2016</b>			Sheet	<b>55</b> of <b>102</b>

		Project Name		Rev
		<b>X556UV</b>		R1.0
<b>Title :</b> <b>Sensors</b>				
Size Custom	<b>Dept.:</b> ASUSTeK COMPUTER INC. <b>Engineer:</b> <b>EE</b>			
Date:   Monday, January 04, 2016			Sheet	61           of       102


		Project Name		Rev
		<b>X556UV</b>		R1.0
Title : ****				
Size	Dept.: ASUSTeK COMPUTER INC. Engineer: EE			
C				
Date: Monday, January 04, 2016			Sheet	62 of 102


		Project Name		Rev
		<b>X556UV</b>		R1.0
<b>Title :</b> <b>VGA_****</b>				
Size	<b>Dept.:</b> <b>ASUSTeK COMPUTER INC.</b> <b>Engineer:</b> <b>EE</b>			
C				
Date:   Monday, January 04, 2016			Sheet	79                      of                      102


		Project Name		Rev
		<b>X556UV</b>		R1.0
<b>Title :</b> <b>VGA_****</b>				
Size	<b>Dept.:</b> <b>ASUSTeK COMPUTER INC.</b> <b>Engineer:</b> <b>EE</b>			
C				
Date:   Monday, January 04, 2016			Sheet	78                      of                      102

		Project Name		Rev
		<b>X556UV</b>		R1.0
<b>Title :</b> <b>NFC</b>				
Size Custom	<b>Dept.:</b> <b>ASUSTeK COMPUTER INC.</b> <b>Engineer:</b> <b>EE</b>			
Date:    Monday, January 04, 2016			Sheet	63      of      102



		Project Name		Rev
		<b>X556</b>		R1.0
<b>Title :</b> <b>NFC</b>				
Size Custom	<b>Dept.:</b> <b>ASUSTeK COMPUTER INC.</b> <b>Engineer:</b> <b>EE</b>			
Date: <b>Monday, January 04, 2016</b>			Sheet	64      of      102

		Project Name		Rev
		<b>X556</b>		R1.0
<b>Title :</b> <b>NFC</b>				
Size Custom	<b>Dept.:</b> <b>ASUSTeK COMPUTER INC.</b> <b>Engineer:</b> <b>EE</b>			
Date: <b>Monday, January 04, 2016</b>			Sheet <b>66</b>	of <b>102</b>

		Project Name		Rev
		<b>X556UV</b>		R1.0
<b>Title :</b> <b>LED indicator</b>				
Size	<b>Dept.:</b> <b>ASUSTeK COMPUTER INC.</b> <b>Engineer:</b> <b>EE</b>			
C				
Date: <b>Monday, January 04, 2016</b>			Sheet	67      of      102